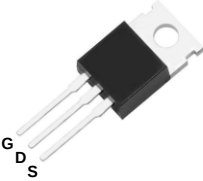
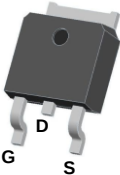
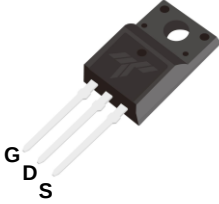
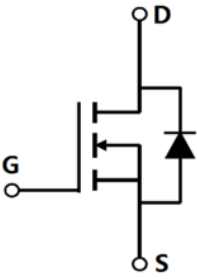


N-channel 80V, 9.5mΩ typ., 68A
 SGT MOSFET S2 in TO-220, TO-251, TO-252, TO-263 and TO-220F

Datasheet - production data

1. Descriptions

TO-220	TO-251
	
TO-252	TO-220F
	
TO-263	Schematic Diagram
	

Key Performance Parameters

Parameters	Value	Unit
BV_{DSS}	80	V
$R_{DS(on),max}$	12	mΩ
$Q_{g,typ}$	43	nC
$I_{D,pulse}$	148	A
E_{AS}	180	mJ

Features

- Extremely low losses due to very low FOM $R_{DS(on)} \cdot Q_g$.
- High-speed switching.
- Qualified for industrial grade applications according to JEDEC.
- 100% UIS Tested.

Applications

High-Efficiency DC-DC Converters, Switching Voltage Regulators and Motor Drivers.

Type/Ordering Code	Package	Marking	Related Links
CSP120N08S2	TO-220	120N08S2	see Appendix A
CSI120N08S2	TO-251		
CSD120N08S2	TO-252		
CSB120N08S2	TO-263		
CSA120N08S2	TO-220F		

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3.	Thermal Characteristics	4
4.	Electrical Characteristics	5
5.	Electrical Characteristics Diagrams	6
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2. Maximum Ratings

at $T_j = 25^\circ\text{C}$, unless otherwise specified

Table 1. Absolute Maximum Ratings

Symbol	Parameter	Values			Unit	Test Condition
		Min.	Typ.	Max.		
V_{DS}	Drain-source voltage ¹⁾	-	-	80	V	$V_{GS}=0V$, $I_D=250\mu A$
I_D	Continuous drain current ²⁾	-	-	68	A	$T_C=25^\circ\text{C}$
$I_{D,pulse}$	Pulsed drain current	-	-	148	A	$T_C=25^\circ\text{C}$
E_{AS}	Avalanche energy, single pulse ³⁾	-	-	180	mJ	$I_D=30A$; $V_{DD}=50V$
I_{AS}	Avalanche current	-	-	30	A	-
V_{GS}	Gate source voltage	-20	-	20	V	static; AC ($f>1\text{ Hz}$)
P_{tot}	Power dissipation (Non FullPAK) TO-220, TO-251, TO-252, TO-263	-	-	75	W	$T_C=25^\circ\text{C}$
P_{tot}	Power dissipation (FullPAK) TO-220F	-	-	27.5	W	$T_C=25^\circ\text{C}$
T_j, T_{stg}	Operating and storage temperature	-55	-	175	$^\circ\text{C}$	-
I_S	Continuous diode forward current	-	-	68	A	$T_C=25^\circ\text{C}$
$I_{S,pulse}$	Diode pulse current ²⁾	-	-	148	A	$T_C=25^\circ\text{C}$

1) Limited by T_j max. Maximum duty cycle $D=0.75$.

2) Pulse width t_p limited by $T_{j,max}$.

3) $V_{DD}=50V$, $L=0.4mH$, $R_G=25\Omega$, Starting $T_j=25^\circ\text{C}$.

3. Thermal Characteristics

Table 2. Thermal Characteristics (Non FullPAK) TO-220, TO-251, TO-252, TO-263

Symbol	Parameter	Values			Unit	Test Condition
		Min.	Typ.	Max.		
R_{thJC}	Thermal resistance, junction - case	-	-	2	°C/W	$T_C = 25^{\circ}\text{C}$
R_{thJA}	Thermal resistance, junction - ambient	-	-	62	°C/W	$T_C = 25^{\circ}\text{C}$
T_{sold}	Soldering temperature, wavesoldering only allowed at leads	-	-	260	°C	Lead Temperature (Soldering, 10 sec)

Table 3. Thermal Characteristics (FullPAK) TO-220F

Symbol	Parameter	Values			Unit	Test Condition
		Min.	Typ.	Max.		
R_{thJC}	Thermal resistance, junction - case	-	-	4.5	°C/W	$T_C = 25^{\circ}\text{C}$
R_{thJA}	Thermal resistance, junction - ambient	-	-	62.5	°C/W	$T_C = 25^{\circ}\text{C}$
T_{sold}	Soldering temperature, wavesoldering only allowed at leads	-	-	260	°C	Lead Temperature (Soldering, 10 sec)

4. Electrical Characteristics

at $T_j = 25^\circ\text{C}$, unless otherwise specified

Table 4. Static Characteristics

Symbol	Parameter	Values			Unit	Test Condition
		Min.	Typ.	Max.		
$V_{(BR)DSS}$	Drain-source breakdown voltage	80	-	-	V	$V_{GS}=0V, I_D=250\mu A$
$V_{(GS)th}$	Gate threshold voltage	1.0	1.8	2.5	V	$V_{DS}=V_{GS}, I_D=250\mu A$
I_{DSS}	Zero gate voltage drain current	-	-	1	μA	$V_{DS}=80V, V_{GS}=0V, T_j=25^\circ C$
I_{GSS}	Gate-source leakage current	-	-	± 100	nA	$V_{GS}=\pm 20V, V_{DS}=0V$
$R_{DS(on)}$	Drain-source on-state resistance	-	9.5	12	m Ω	$V_{GS}=10V, I_D=15A, T_j=25^\circ C$
R_G	Gate resistance	-	1.9	-	Ω	$V_{DD}=0V, V_{GS}=0V, F=1MHz$
g_{fs}	Transconductance		40		S	$V_{DS}=5V, I_D=15A$

Table 5. Dynamic Characteristics

Symbol	Parameter	Values			Unit	Test Condition
		Min.	Typ.	Max.		
C_{iss}	Input capacitance	-	1450	-	pF	$V_{GS}=0V, V_{DS}=40V, f=1MHz$
C_{oss}	Output capacitance	-	209	-	pF	$V_{GS}=0V, V_{DS}=40V, f=1MHz$
C_{rss}	Reverse transfer capacitance	-	4.0	-	pF	$V_{GS}=0V, V_{DS}=40V, f=1MHz$
$t_{d(on)}$	Turn-on delay time	-	19	-	ns	$V_{DD}=40V, V_{GS}=10V, I_D=14.5A, R_G=3\Omega$
t_r	Rise time	-	10	-	ns	$V_{DD}=40V, V_{GS}=10V, I_D=14.5A, R_G=3\Omega$
$t_{d(off)}$	Turn-off delay time	-	24.6	-	ns	$V_{DD}=40V, V_{GS}=10V, I_D=14.5A, R_G=3\Omega$
t_f	Fall time	-	5	-	ns	$V_{DD}=40V, V_{GS}=10V, I_D=14.5A, R_G=3\Omega$

Table 6. Gate Charge Characteristics

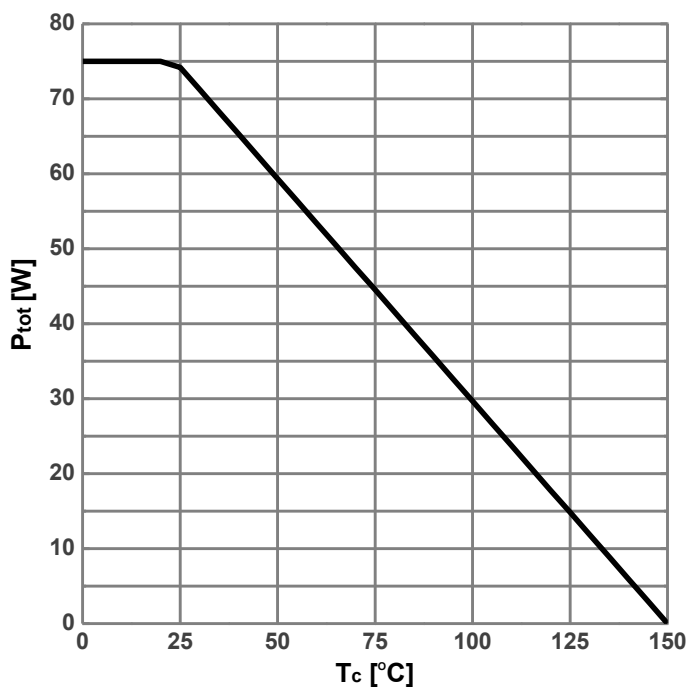
Symbol	Parameter	Values			Unit	Test Condition
		Min.	Typ.	Max.		
Q_{gs}	Gate to source charge	-	6.4	-	nC	$V_{DD}=40V, I_D=14.5A, V_{GS}=0 \text{ to } 10V$
Q_{gd}	Gate to drain charge	-	3.2	-	nC	$V_{DD}=40V, I_D=14.5A, V_{GS}=0 \text{ to } 10V$
Q_g	Gate charge total	-	26	-	nC	$V_{DD}=40V, I_D=14.5A, V_{GS}=0 \text{ to } 10V$
$V_{plateau}$	Gate plateau voltage	-	5.0	-	V	$V_{DD}=40V, I_D=14.5A, V_{GS}=0 \text{ to } 10V$

Table 7. Reverse Diode Characteristics

Symbol	Parameter	Values			Unit	Test Condition
		Min.	Typ.	Max.		
V_{SD}	Diode forward voltage	-	0.82	-	V	$V_{GS}=0V, I_F=15A, T_j=25^\circ C$
t_{rr}	Reverse recovery time	-	17	-	ns	$V_R=40V, I_F=10A, di_F/dt=100A/\mu s$
Q_{rr}	Reverse recovery charge	-	64	-	μC	$V_R=40V, I_F=10A, di_F/dt=100A/\mu s$
I_{rrm}	Peak reverse recovery current	-	19	-	A	$V_R=40V, I_F=10A, di_F/dt=100A/\mu s$

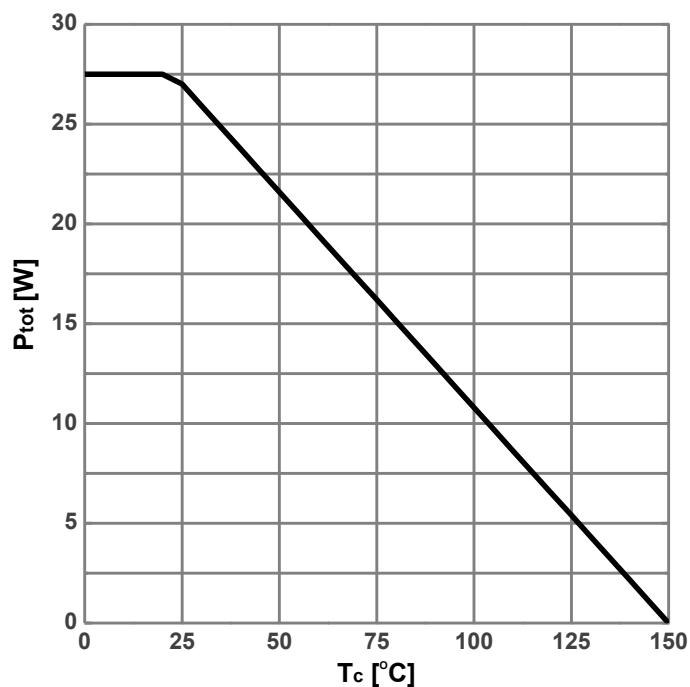
5. Electrical Characteristics Diagrams

Diagram 1: Power dissipation (Non FullPAK)



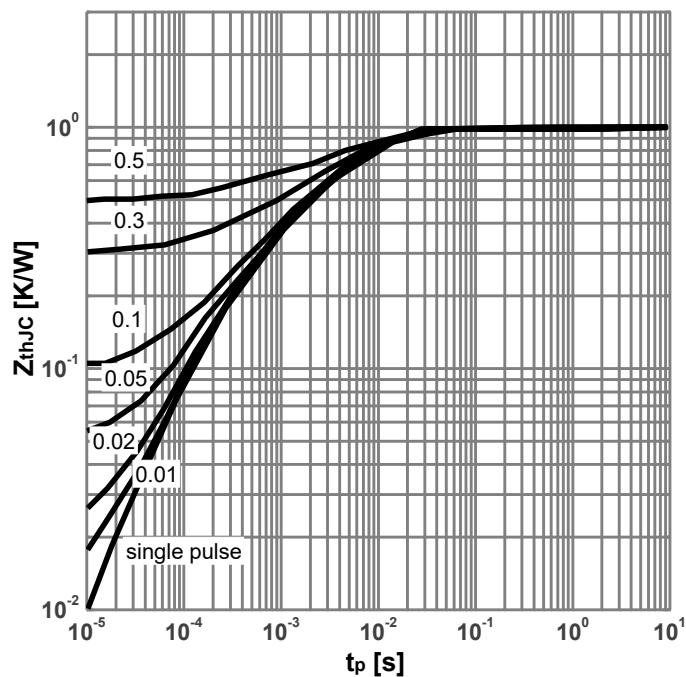
$$P_{tot}=f(T_c)$$

Diagram 2: Power dissipation (FullPAK)



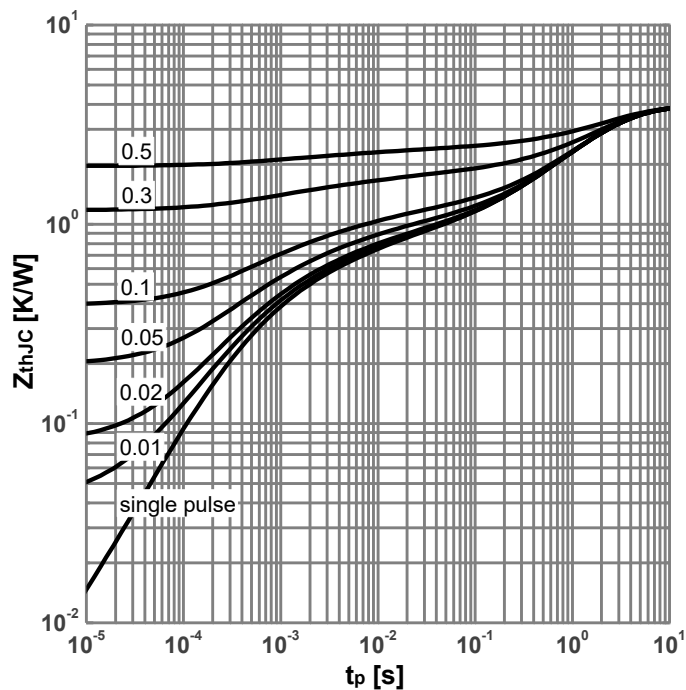
$$P_{tot}=f(T_c)$$

Diagram 3: Max. transient thermal impedance (Non FullPAK)



$$Z_{thJC}=f(t_p); \text{ parameter: } D= t_p/T$$

Diagram 4: Max. transient thermal impedance (FullPAK)



$$Z_{thJC}=f(t_p); \text{ parameter: } D= t_p/T$$

Diagram 5: Safe operating area (Non FullPAK)

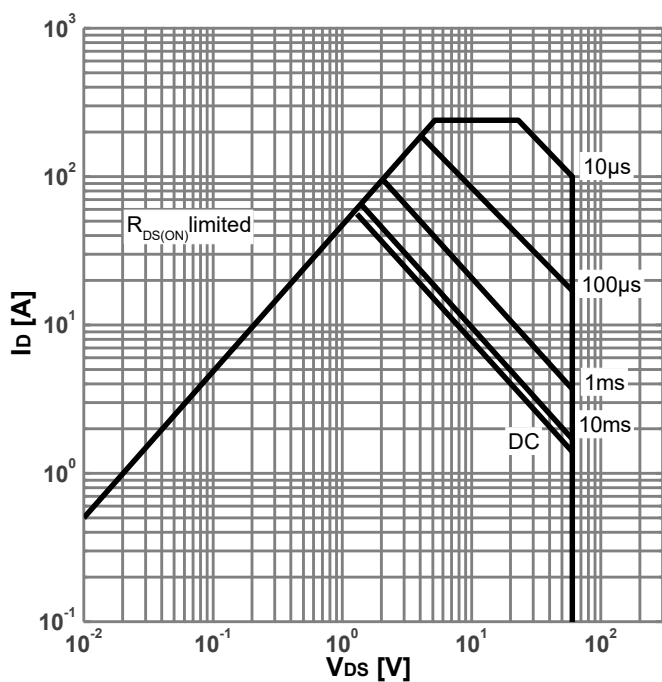

 $I_D = f(V_{DS}); T_J = 25^\circ\text{C}; D = 0; \text{parameter: } t_p$

Diagram 6: Safe operating area (FullPAK)

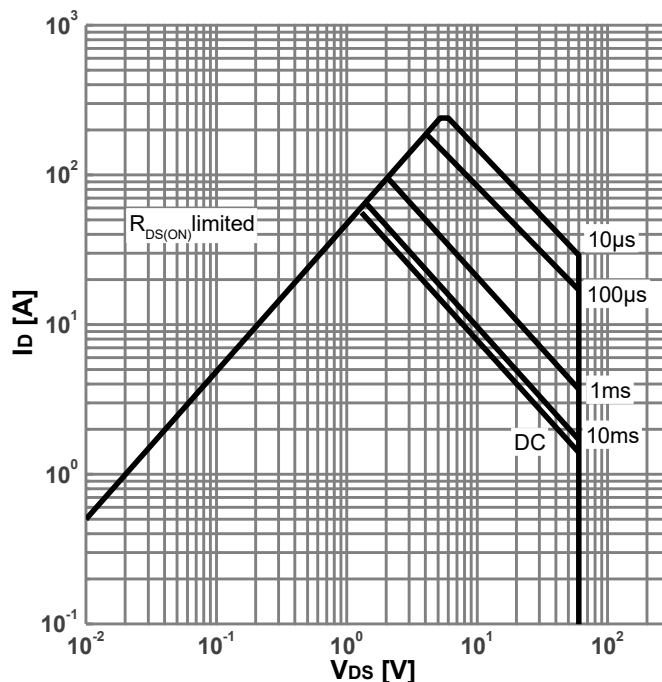

 $I_D = f(V_{DS}); T_J = 25^\circ\text{C}; D = 0; \text{parameter: } t_p$

Diagram 7: Typ. output characteristics

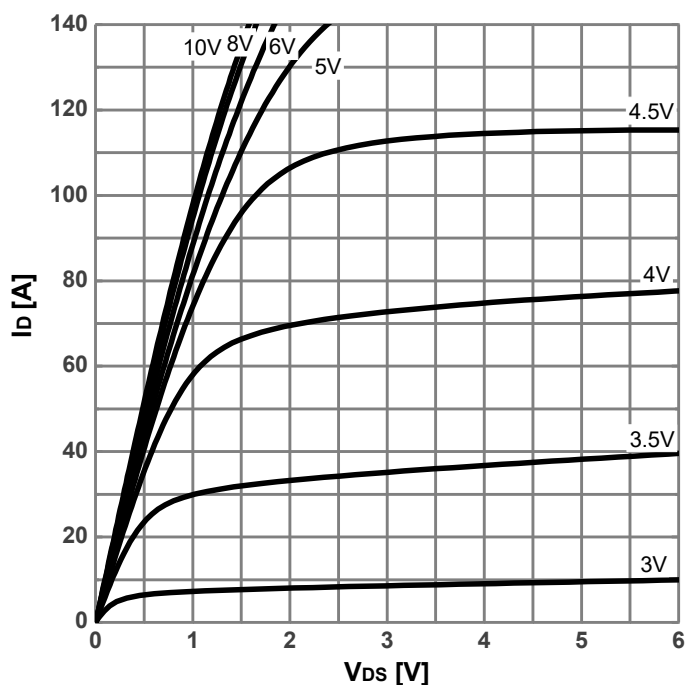

 $I_D = f(V_{DS}); T_J = 25^\circ\text{C}; \text{parameter: } V_{GS}$

Diagram 8: Typ. output characteristics

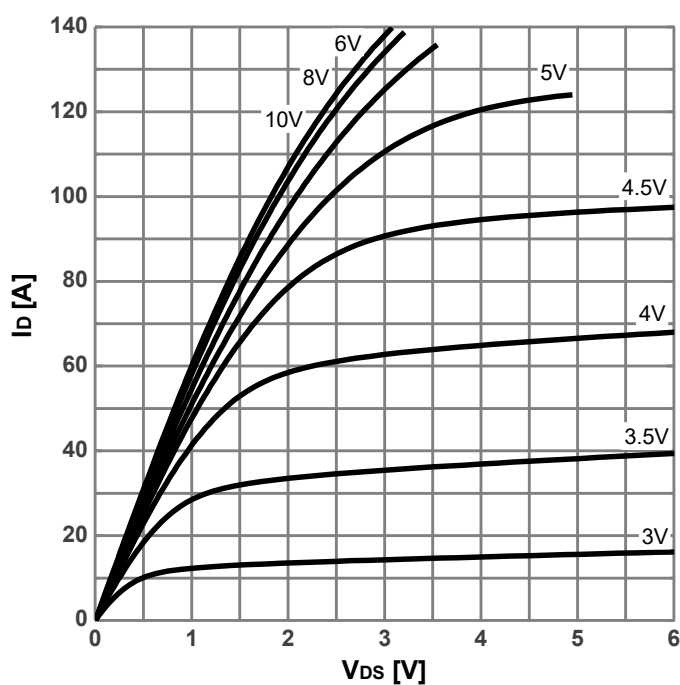

 $I_D = f(V_{DS}); T_J = 125^\circ\text{C}; \text{parameter: } V_{GS}$

Diagram 9: Typ. transfer characteristics

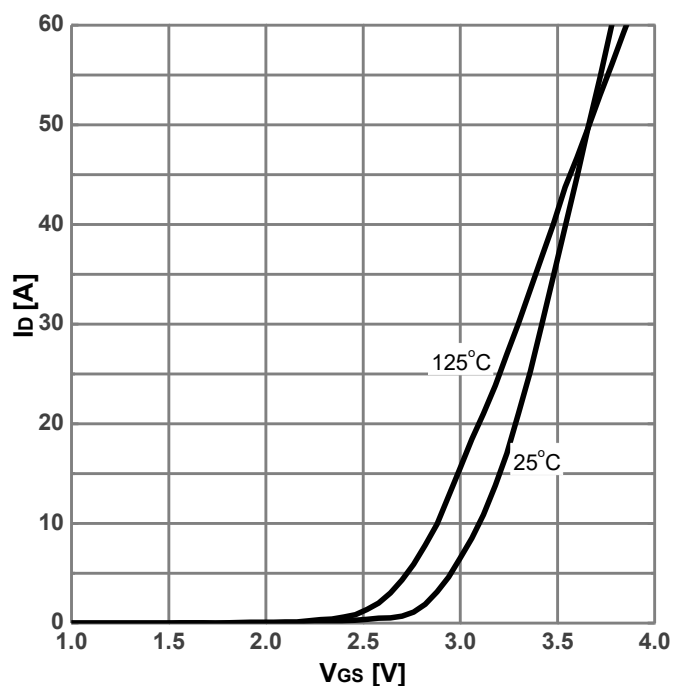

 $I_D = f(V_{GS}); V_{DS} = 15V; \text{parameter: } T_j$

Diagram 10: Gate threshold voltage vs. Junction temperature

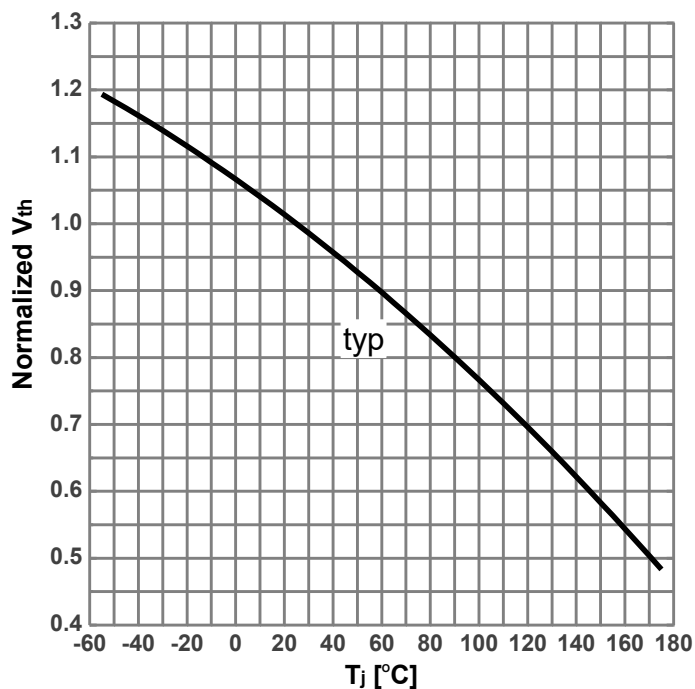

 $V_{th} = f(T_j); I_D = 250\mu A$

Diagram 11: On-state resistance vs. Drain current

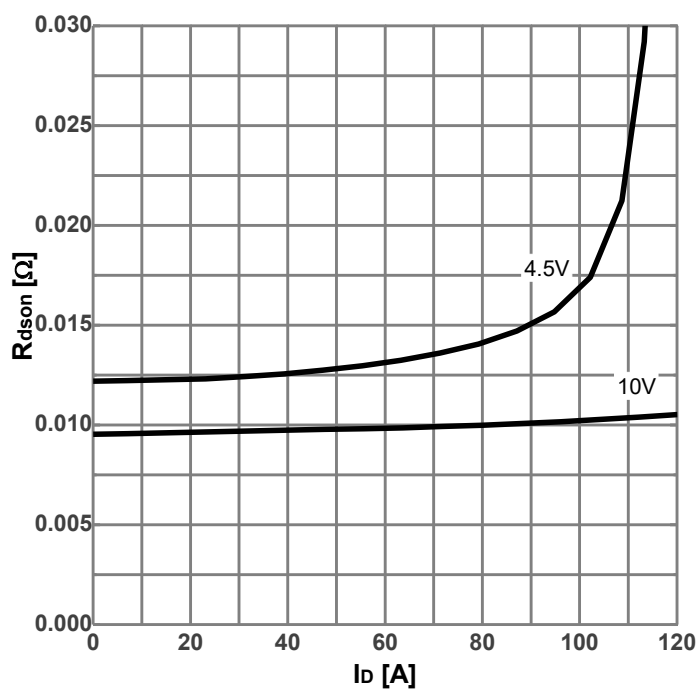

 $R_{DS(on)} = f(I_D); T_j = 25^\circ C; \text{parameter: } V_{GS}$

Diagram 12: On-state resistance vs. Junction temperature

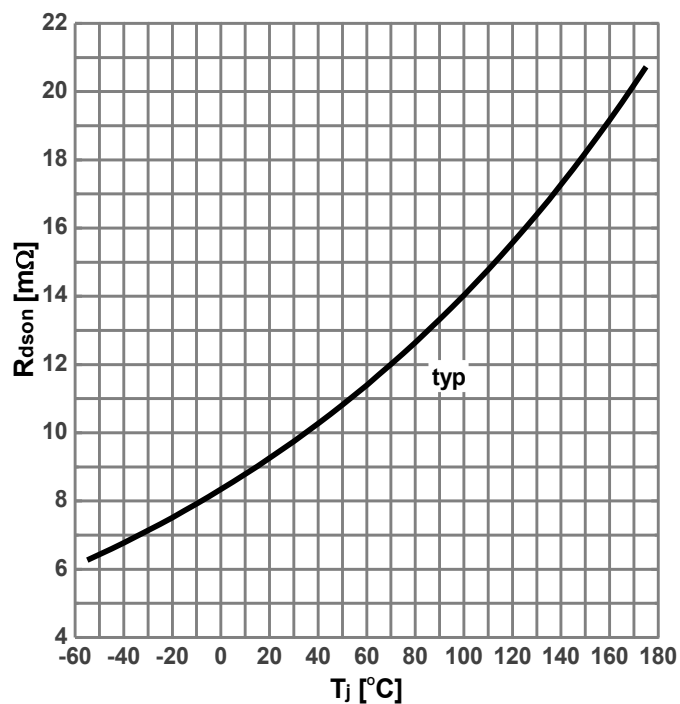
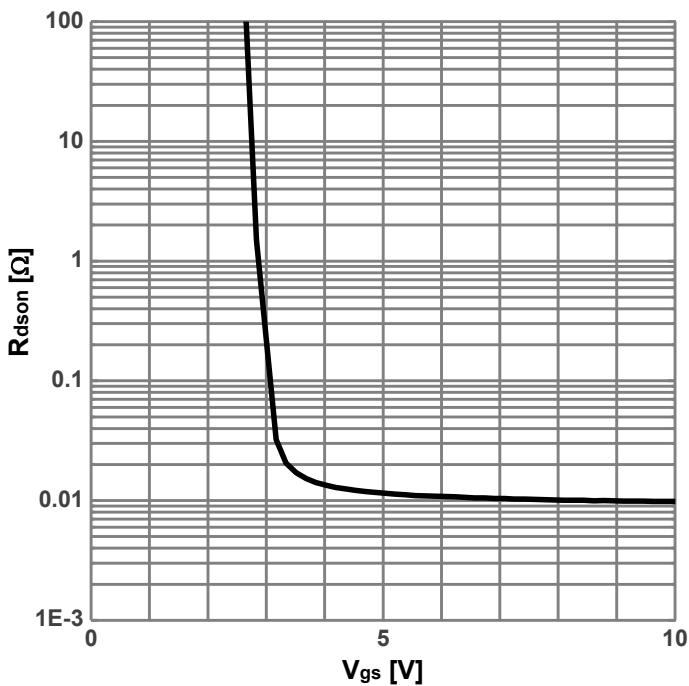
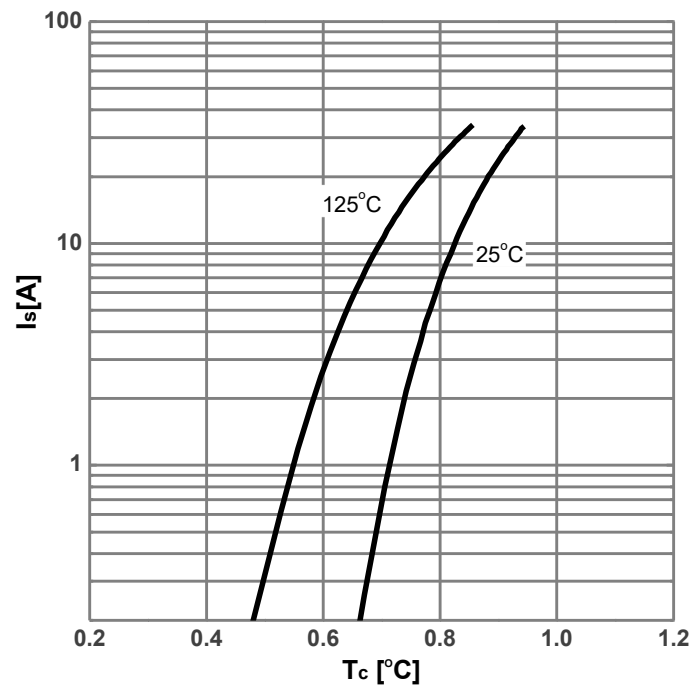

 $R_{DS(on)} = f(T_j); I_D = 15A; V_{GS} = 10V$

Diagram 13: On-state resistance vs. Vgs characteristics



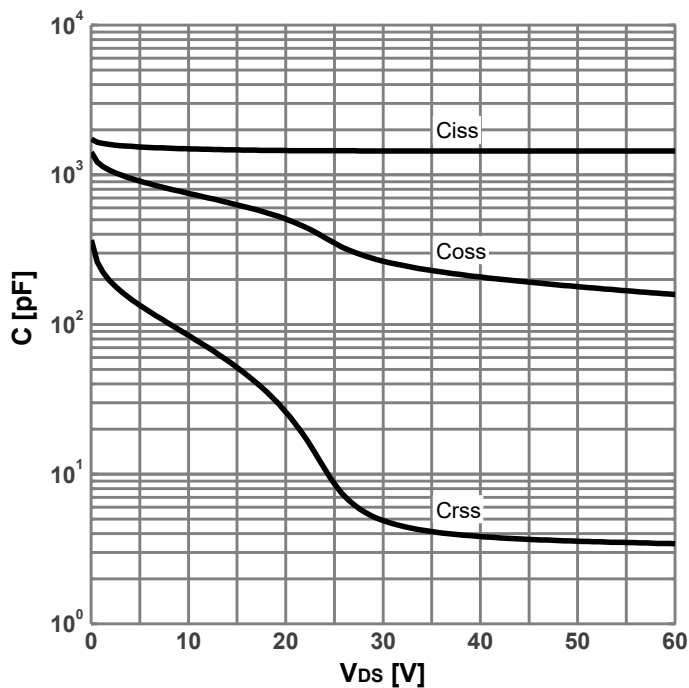
$R_{DS(on)}=f(V_{gs}); T_J=25^{\circ}C; I_D=15A$

Diagram 14: Forward characteristics of reverse diode



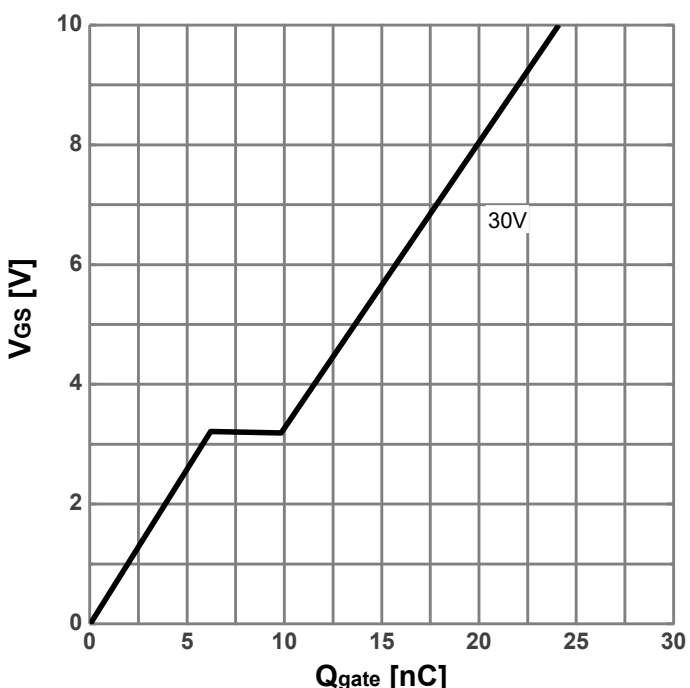
$I_F=f(V_{SD});$ parameter: T_J

Diagram 15: Typ. capacitances



$C=f(V_{DS}); V_{GS}=0V; f=1MHz$

Diagram 16: Typ. gate charge



$V_{GS}=f(Q_{gate}); I_D=14.5A$ pulsed; $V_{DS}=30V$

6. Test Circuits

Table 7. Diode Characteristics

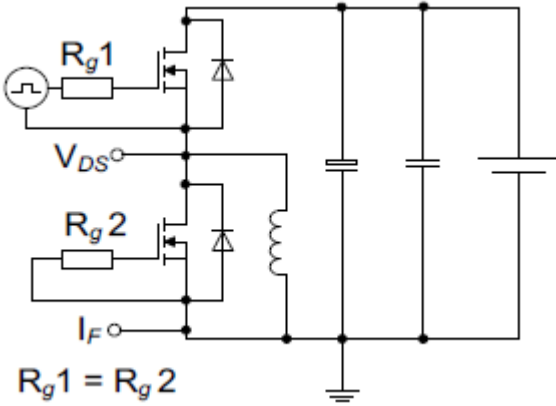
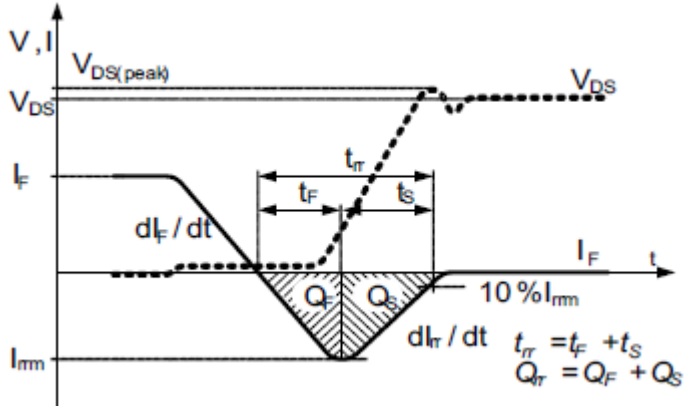
Test circuit for diode characteristics	Diode recovery waveform
	

Table 8. Switching Times

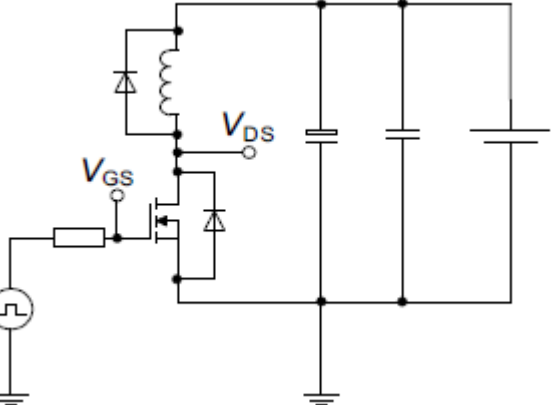
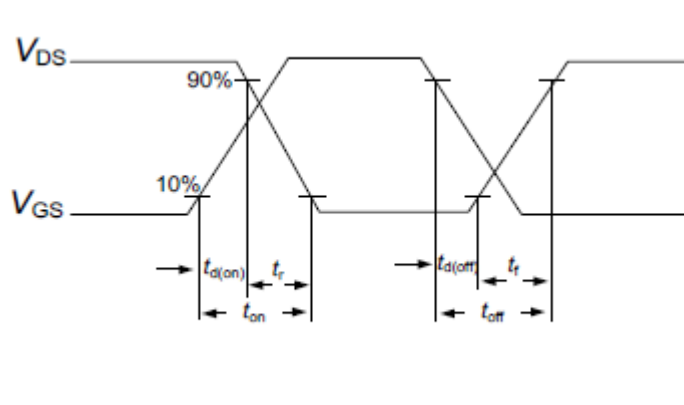
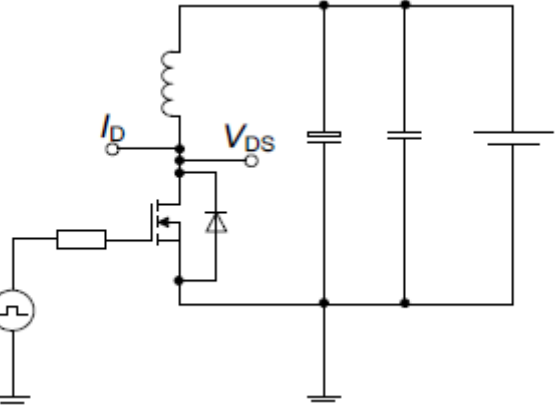
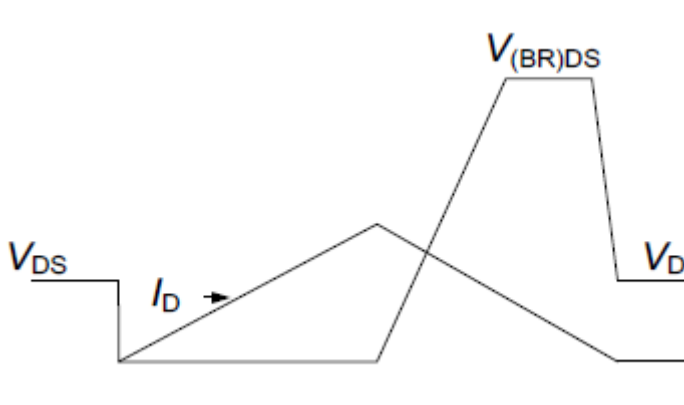
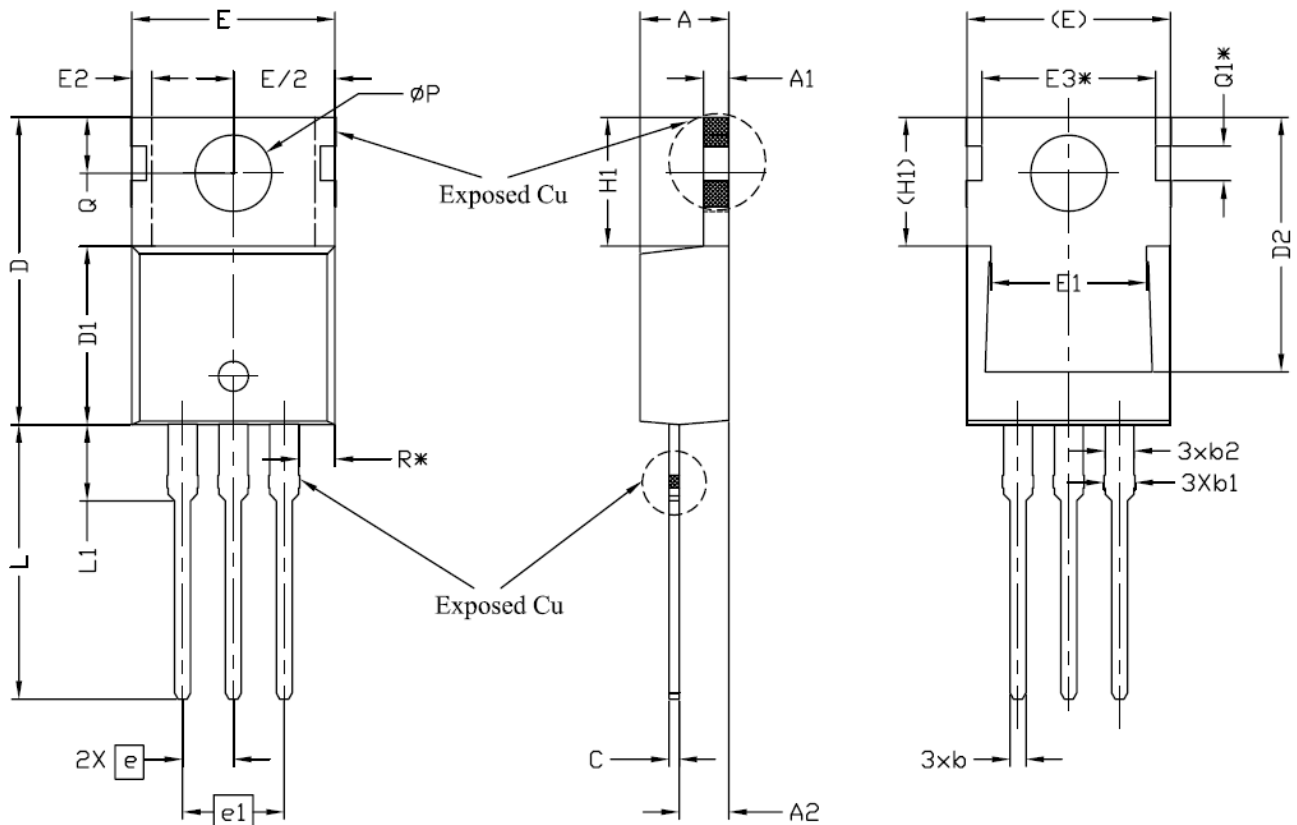
Switching times test circuit for inductive load	Switching times waveform
	

Table 9. Unclamped Inductive Load

Unclamped inductive load test circuit	Unclamped inductive waveform
	

7. Package Outlines

Figure 1 Outline TO-220 Dimensions in mm



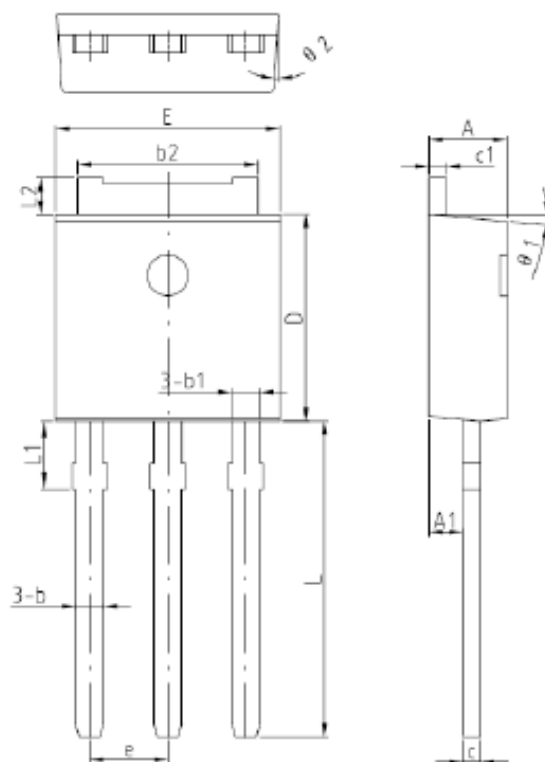
SYMBOL	DIMENSIONS			NOTES
	MIN.	NOM.	MAX.	
A	4.24	4.44	4.64	
A1	1.15	1.27	1.40	
A2	2.30	2.48	2.70	
b	0.70	0.80	0.90	
b1	1.20	1.55	1.75	
b2	1.20	1.45	1.70	
c	0.40	0.50	0.60	
D	14.70	15.37	16.00	4
D1	8.82	8.92	9.02	
D2	12.43	12.73	12.83	5
E	9.96	10.16	10.36	4,5
E1	6.86	7.77	8.89	5
E2	-	-	0.76	6
E3*	8.70REF.			
e	2.54BSC			
e1	5.08BSC			
H1	6.30	6.45	6.60	5,6
L	13.47	13.72	13.97	
L1	3.60	3.80	4.00	
ØP	3.75	3.84	3.93	
Q	2.60	2.80	3.00	
Q1*	1.73REF.			
R*	1.82REF.			



Note:

1. Package Reference: JEDEC TO220, Variation AB.
2. All Dimensions Are In mm.
3. Slot Required, Notch May Be Rounded
4. Dimension D & E Do Not Include Mold Flash. Mold Flash Shall Not Exceed 0.127mm Pre Side. These Dimensions Are Measured At The Outermost Extreme Of The Plastic Body.
5. Thermal Pad Contour Optional Within Dimensions E, H1, D2 & E1.
6. Dimension E2 & H1 Define A Zone Where Stamping And Singulation Irregularities Are Allowed.
7. "*" is reference .

Figure 2 Outline TO-251 Dimensions in mm



Symbol	Dimensions(mm)		
	Min.	Typ.	Max.
A	2.20	2.30	2.40
A1	0.90	1.01	1.17
b	0.50	-	0.91
b1	-	0.81	-
b2	5.13	5.33	5.46
c	0.46	0.50	0.60
c1	0.46	0.50	0.60
D	5.95	6.10	6.25
E	6.45	6.60	6.75
e	2.286(BSC)		
L	9.00	9.30	9.60
L1	-	2.00	-
L2	0.90	-	1.25
θ1	-	5°	-
θ2	-	3°	-

Figure 3 Outline TO-252 Dimensions in mm

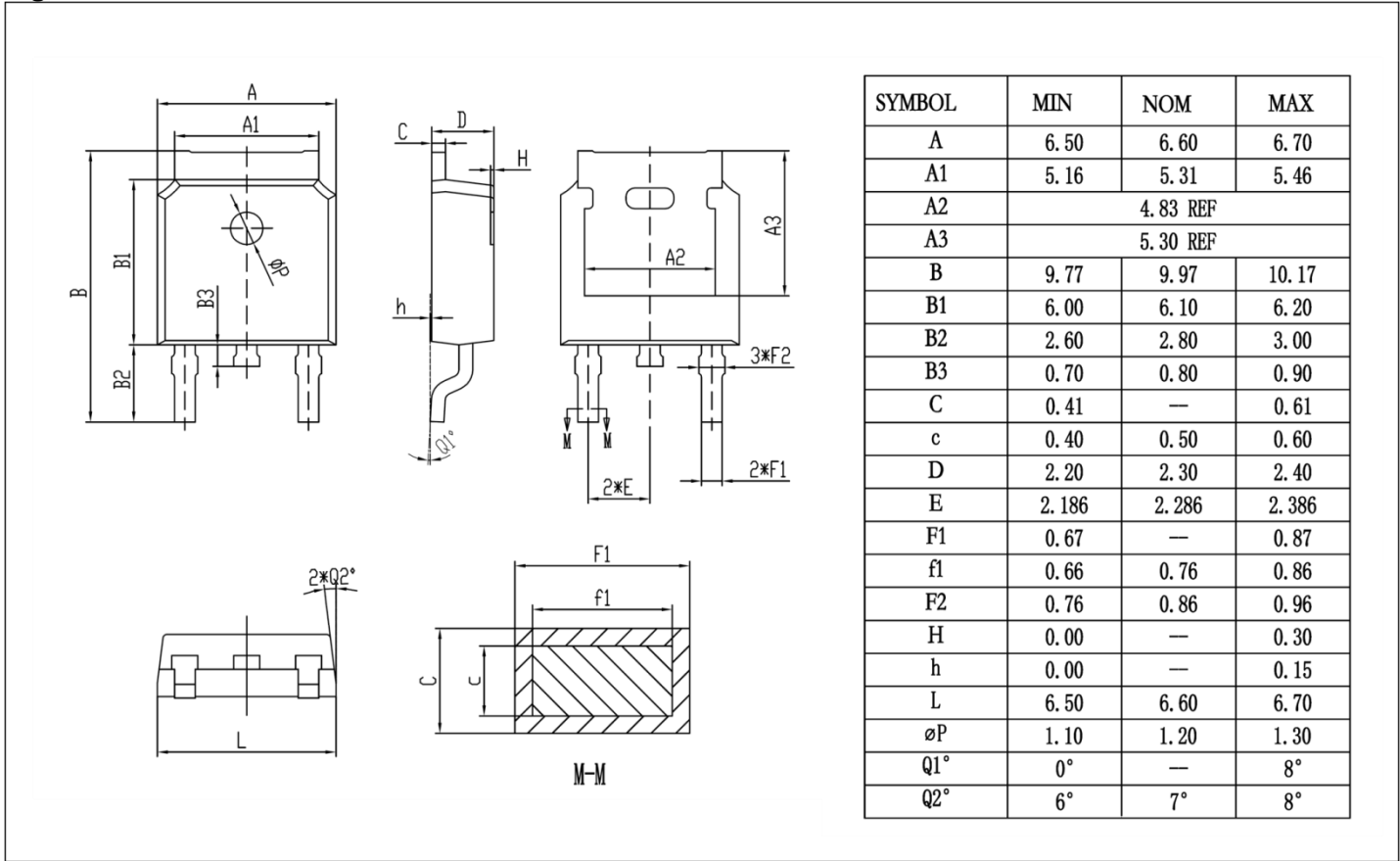
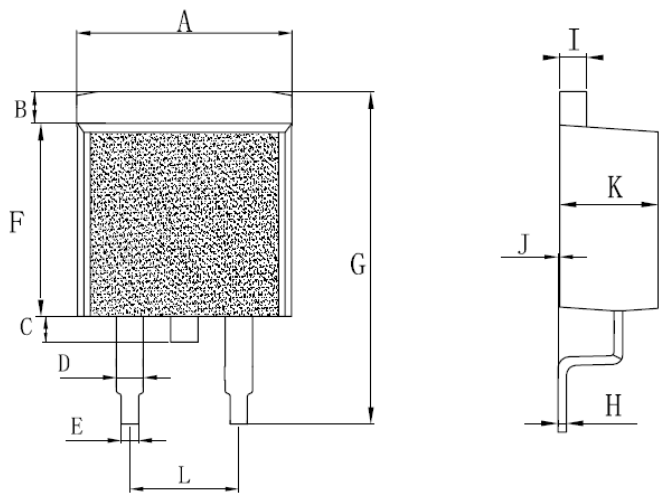


Figure 4 Outline TO-263 Dimensions in mm

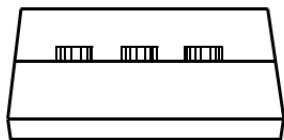
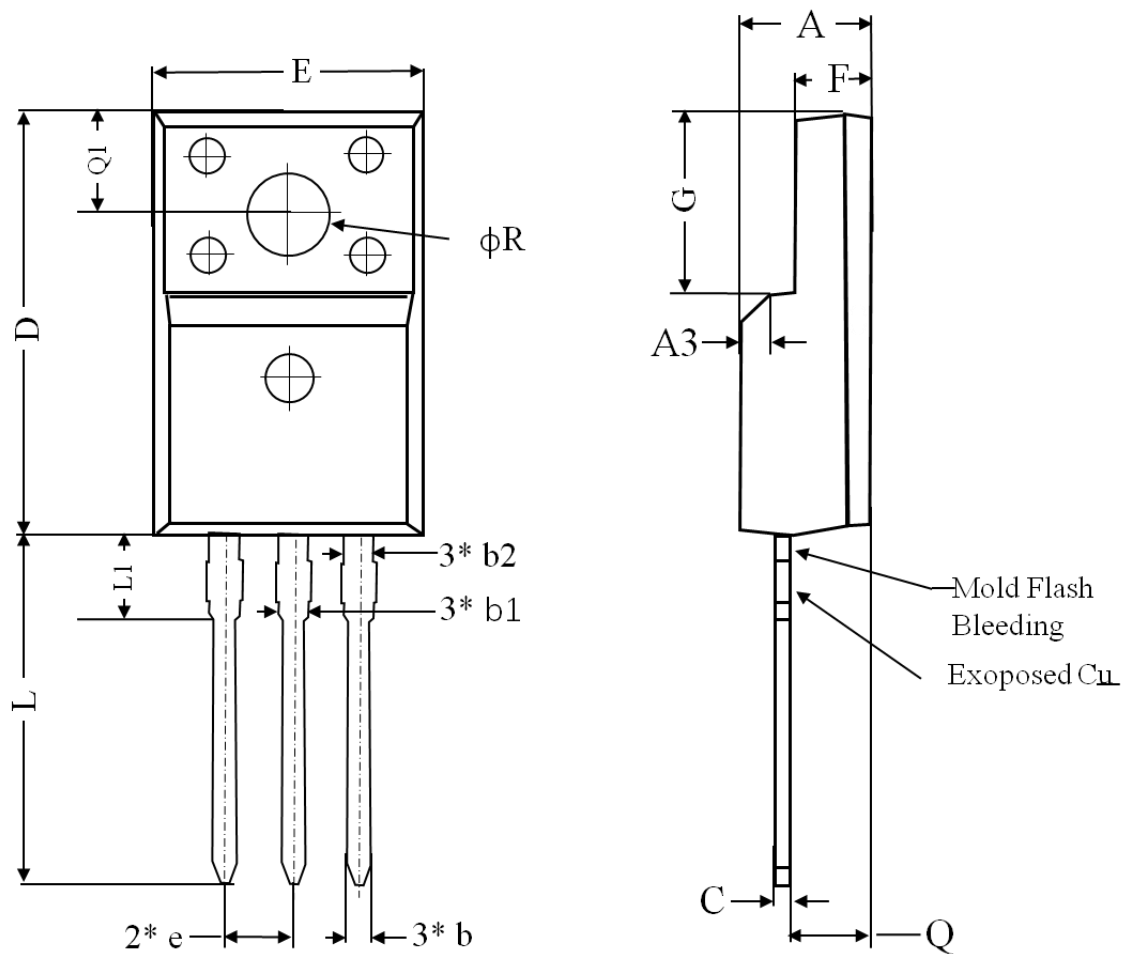
PACKAGE OUTLINE DIMENSIONS

TO-263



DIM.	Unit(mm)		Unit(inch)	
	Min	Max	Min	Max
A	9.7	10.4	0.381	0.409
B	1.31	1.62	0.051	0.063
C	0.65	1.22	0.025	0.048
D	1.15	1.36	0.045	0.053
E	0.62	0.95	0.024	0.037
F	8.75	9.32	0.344	0.366
G	14.75	15.8	0.580	0.622
H	0.32	0.48	0.012	0.018
I	1.18	1.36	0.046	0.053
J	0	0.15	0	0.005
K	4.38	4.86	0.172	0.191
L	4.85	5.23	0.190	0.205

Figure 5 Outline TO-220 FullPAK Dimensions in mm



Note:

1. All Dimension Are In mm.
2. Package Body Sizes Exclude Mold Flash And Burrs Mold Flash Should Be less Than 6 Mil.

SYMBOL	DIMENSIONS		
	Min.	Nom.	Max.
A	4.60	4.70	4.80
b	0.70	0.80	0.91
b1	1.20	1.30	1.47
b2	1.10	1.20	1.30
C	0.45	0.50	0.63
D	15.80	15.87	15.97
e	2.54		
E	10.00	10.10	10.30
F	2.44	2.54	2.64
G	6.50	6.70	6.90
L	12.90	13.10	13.30
L1	3.13	3.23	3.33
Q	2.65	2.75	2.85
Q1	3.20	3.30	3.40
Φr	3.08	3.18	3.28

8. Appendix

CoolSemi Webpage: www.coolsemi.com.