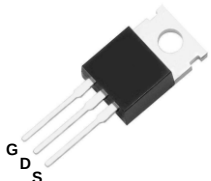
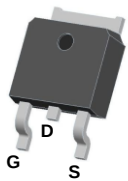
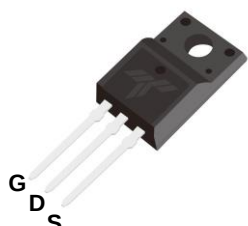
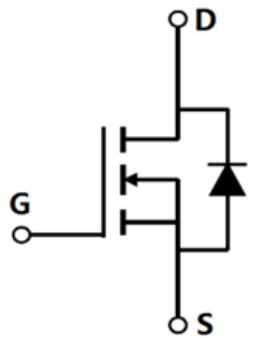


N-channel 60V, 7.5mΩ typ.,
SGT MOSFET S2 in TO-220, TO-251, TO-252 and TO-220F

Datasheet - production data

1. Descriptions

TO-220	TO-251
	
TO-252	TO-220F
	
Schematic Diagram	
	

Key Performance Parameters

Parameters	Value	Unit
BV_{DSS}	60	V
$R_{DS(on),max}$	9	mΩ
P_D	75	W
I_D	60	A

Features

- High Speed Power Switching, Logic level
- Enhanced Body diode dv/dt capability
- Enhanced Avalanche Ruggedness
- 100% UIS Tested, 100% Rg Tested
- Lead Free, Halogen Free

Applications

- DC/DC Converter
- Motor Drivers
- Ideal for high-frequency switching and synchronous rectification

Type/Ordering Code	Package	Marking	Related Links
CSP090N06S2	TO-220	090N06S2	see Appendix A
CSI090N06S2	TO-251		
CSD090N06S2	TO-252		
CSA090N06S2	TO-220F		

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3.	Thermal Characteristics	3
4.	Electrical Characteristics	4
5.	Electrical Characteristics Diagrams	5
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7.	Package Outlines	10
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2. Maximum Ratings

at $T_j = 25^\circ\text{C}$, unless otherwise specified

Absolute Maximum Ratings

Symbol	Parameter	Values			Unit	Test Condition
		Min.	Typ.	Max.		
V_{DS}	Drain-source voltage	-	-	60	V	$V_{GS}=0\text{V}$, $I_D=250\mu\text{A}$
V_{GS}	Gate source voltage	-20	-	20	V	static; AC ($f>1\text{ Hz}$)
I_D	Continuous drain current	-	-	60 43	A	$T_C=25^\circ\text{C}$ $T_C=100^\circ\text{C}$
$I_{D,pulse}$	Pulsed drain current	-	-	240	A	$T_C=25^\circ\text{C}$
P_D	Power dissipation (Non FullPAK) TO-220, TO-251, TO-252	-	-	75	W	$T_C=25^\circ\text{C}$
P_D	Power dissipation (FullPAK) TO-220F	-	-	24	W	$T_C=25^\circ\text{C}$
E_{AS}	Avalanche energy, single pulse ¹⁾	-	-	180	mJ	$I_D=6\text{A}$; $V_{DD}=50\text{V}$
T_j, T_{stg}	Operating and storage temperature	-55	-	175	$^\circ\text{C}$	-

3. Thermal Characteristics

Thermal Characteristics (Non FullPAK) TO-220, TO-251, TO-252

Symbol	Parameter	Values			Unit	Test Condition
		Min.	Typ.	Max.		
R_{thJC}	Thermal resistance, junction - case	-	-	2	$^\circ\text{C/W}$	$T_C = 25^\circ\text{C}$
R_{thJA}	Thermal resistance, junction - ambient	-	-	75	$^\circ\text{C/W}$	$T_C = 25^\circ\text{C}$

Thermal Characteristics (FullPAK) TO-220F

Symbol	Parameter	Values			Unit	Test Condition
		Min.	Typ.	Max.		
R_{thJC}	Thermal resistance, junction - case	-	-	6.25	$^\circ\text{C/W}$	$T_C = 25^\circ\text{C}$
R_{thJA}	Thermal resistance, junction - ambient ²⁾	-	-	75	$^\circ\text{C/W}$	$T_C = 25^\circ\text{C}$

4. Electrical Characteristics

at $T_J = 25^\circ\text{C}$, unless otherwise specified

Symbol	Parameter	Values			Unit	Test Condition
		Min.	Typ.	Max.		

Off Characteristics

$V_{(BR)DSS}$	Drain-source breakdown voltage	60	-	-	V	$V_{GS}=0V, I_D=250\mu A$
I_{DSS}	Zero gate voltage drain current	-	-	1	μA	$V_{DS}=60V, V_{GS}=0V$
I_{GSS}	Gate-source leakage current	-	-	± 100	nA	$V_{GS}=\pm 20V, V_{DS}=0V$

On Characteristics³⁾

$V_{(GS)th}$	Gate threshold voltage	1.0	1.8	2.5	V	$V_{DS}=V_{GS}, I_D=250\mu A$
$R_{DS(on)}$	Drain-source on-state resistance	-	7.5 10	9 14	m Ω	$V_{GS}=10V, I_D=20A$ $V_{GS}=4.5V, I_D=10A$
R_G	Gate resistance	-	2.6	-	Ω	$V_{DD}=0V, V_{GS}=0V, F=1MHz$
g_{fs}	Transconductance	-	80	-	S	$V_{DS}=5V, I_D=20A$

Dynamic Characteristics

C_{iss}	Input capacitance	-	1480	-	pF	$V_{GS}=0V, V_{DS}=30V,$ $F=1MHz$
C_{oss}	Output capacitance	-	290	-	pF	
C_{rss}	Reverse transfer capacitance	-	4.1	-	pF	

Switching Characteristics⁴⁾

$t_{d(on)}$	Turn-on delay time	-	11	-	ns	$V_{DD}=30V, V_{GS}=10V,$ $I_D=14.5A, R_G=3\Omega$
t_r	Turn-on rise time	-	5	-	ns	
$t_{d(off)}$	Turn-off delay time	-	56	-	ns	
t_f	Turn-off fall time	-	12	-	ns	
Q_g	Gate charge total	-	23	-	nC	$V_{DD}=30V, I_D=14.5A, V_{GS}=10V$
Q_{gs}	Gate to source charge	-	4.8	-	nC	
Q_{gd}	Gate to drain charge	-	2.4	-	nC	

Reverse Diode Characteristics

V_{SD}	Diode forward voltage ³⁾	-	0.9	1.2	V	$V_{GS}=0V, I_F=20A$
I_S	Diode forward current ²⁾	-	-	60	A	
t_{rr}	Reverse recovery time	-	32	-	ns	$V_{GS}=0V, I_F=14.5A,$ $di/dt=100A/\mu s^3)$
Q_{rr}	Reverse recovery charge	-	46	-	nC	

1) $V_{DD}=50V, L=10mH, R_G=25\Omega$, Starting $T_J=25^\circ\text{C}$.

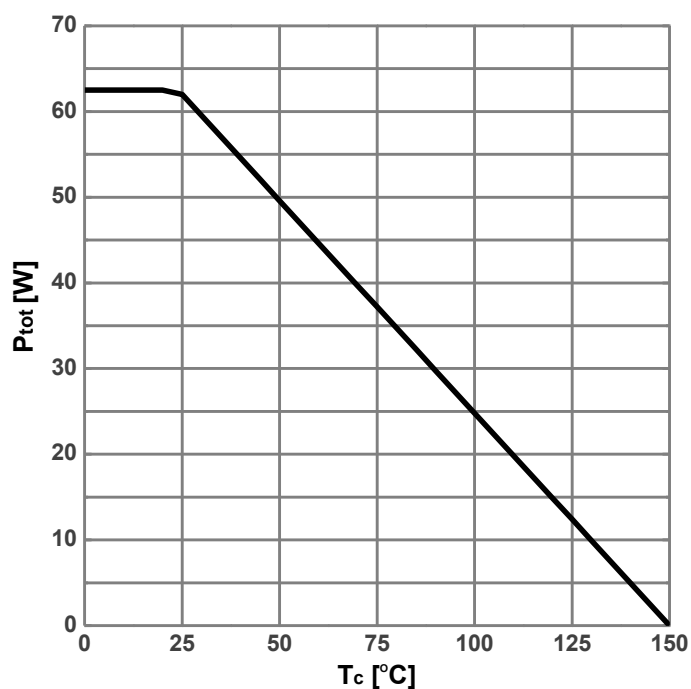
2) Surface Mounted on FR4 Board, $t \leq 10$ sec.

3) Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.

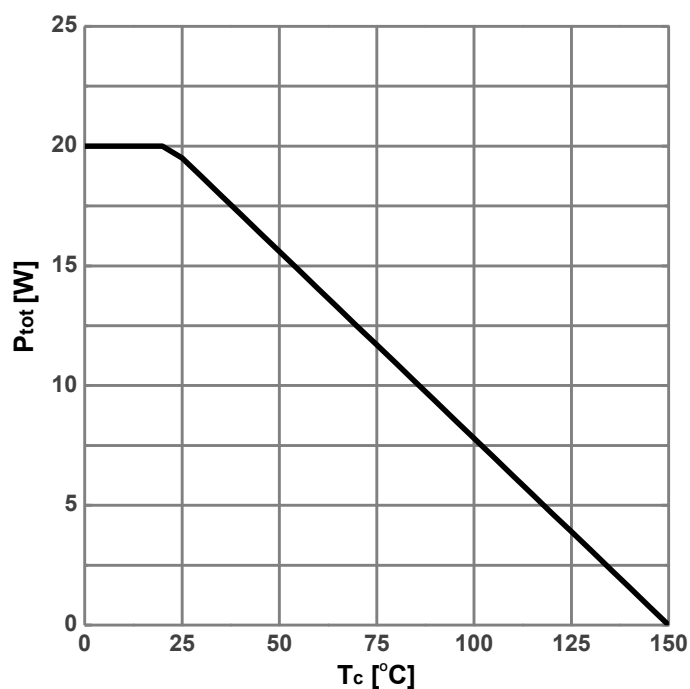
4) Guaranteed by design, not subject to production

5) Repetitive Rating: Pulse width limited by maximum junction temperature.

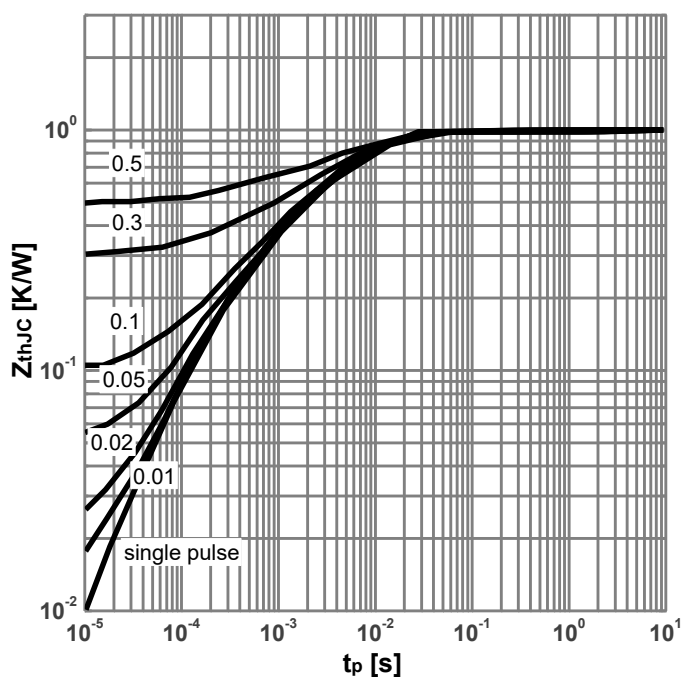
5. Electrical Characteristics Diagrams

Diagram 1: Power dissipation (Non FullPAK)


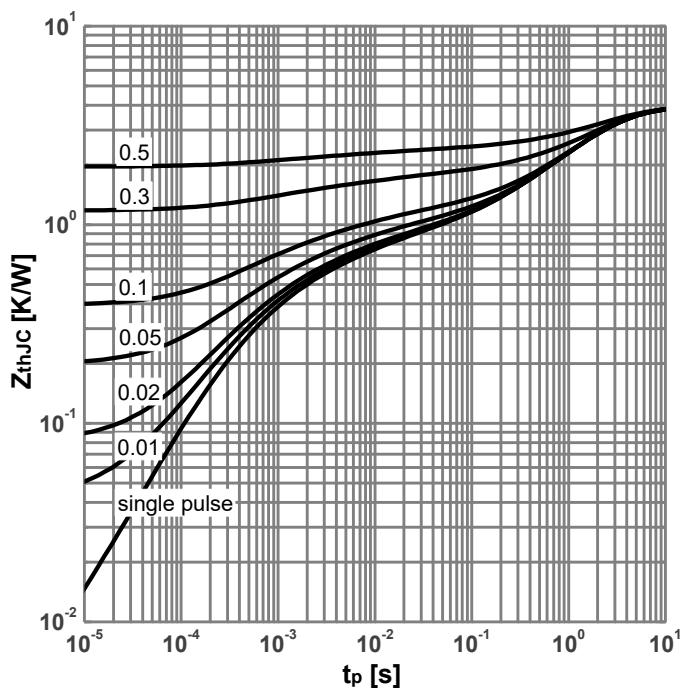
$$P_{tot}=f(T_c)$$

Diagram 2: Power dissipation (FullPAK)


$$P_{tot}=f(T_c)$$

Diagram 3: Max. transient thermal impedance (Non FullPAK)


$$Z_{thJC}=f(t_p); \text{ parameter: } D= t_p/T$$

Diagram 4: Max. transient thermal impedance (FullPAK)


$$Z_{thJC}=f(t_p); \text{ parameter: } D= t_p/T$$

Diagram 5: Safe operating area (Non FullPAK)

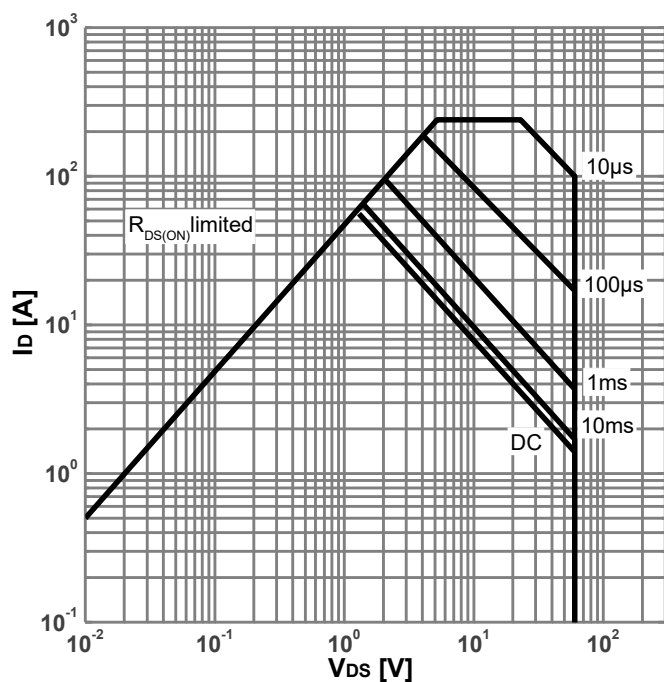

 $I_D = f(V_{DS}); T_J = 25^\circ\text{C}; D = 0; \text{parameter: } t_p$

Diagram 6: Safe operating area (FullPAK)

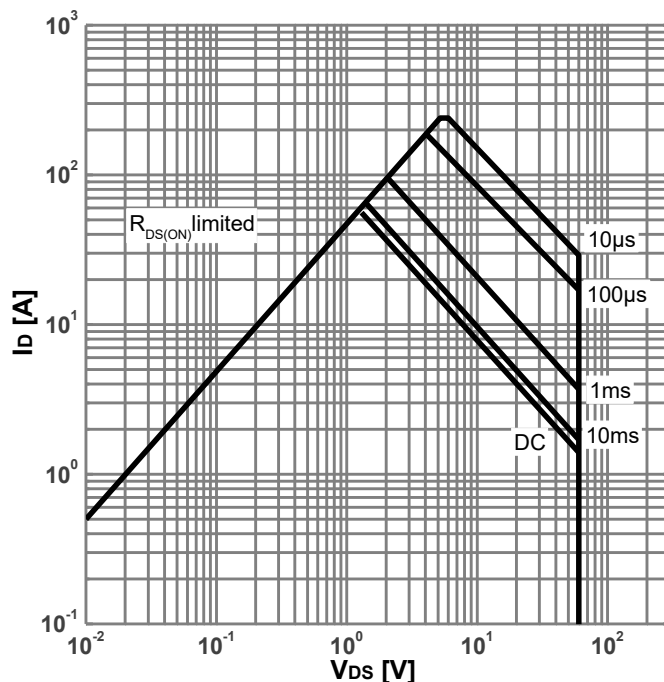

 $I_D = f(V_{DS}); T_J = 25^\circ\text{C}; D = 0; \text{parameter: } t_p$

Diagram 7: Typ. output characteristics

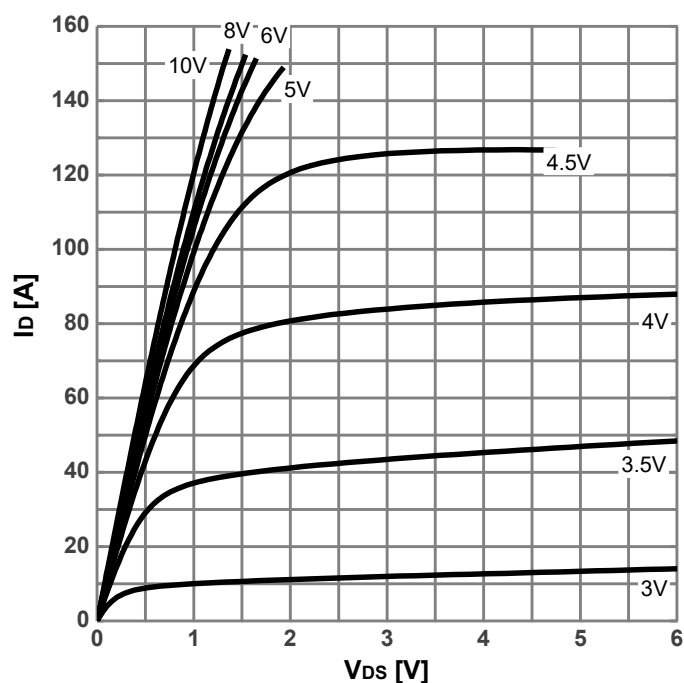

 $I_D = f(V_{DS}); T_J = 25^\circ\text{C}; \text{parameter: } V_{GS}$

Diagram 8: Typ. output characteristics

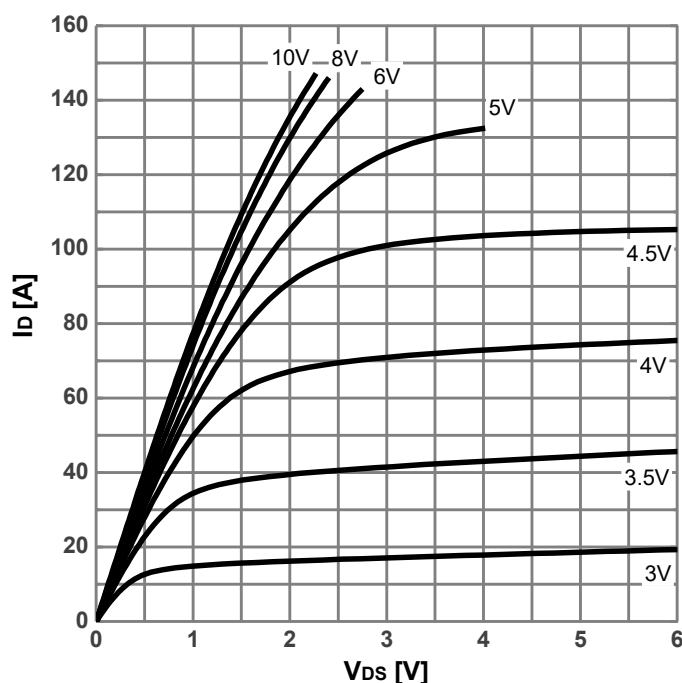
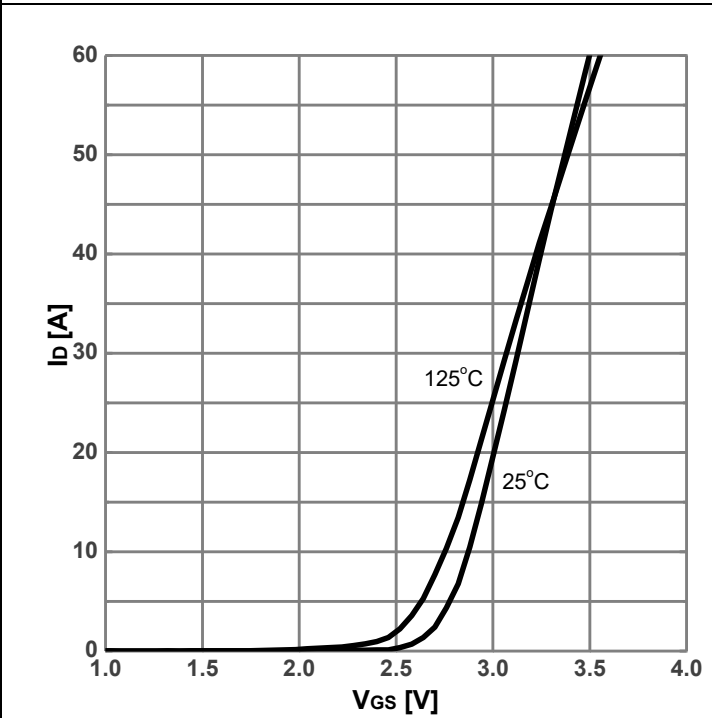
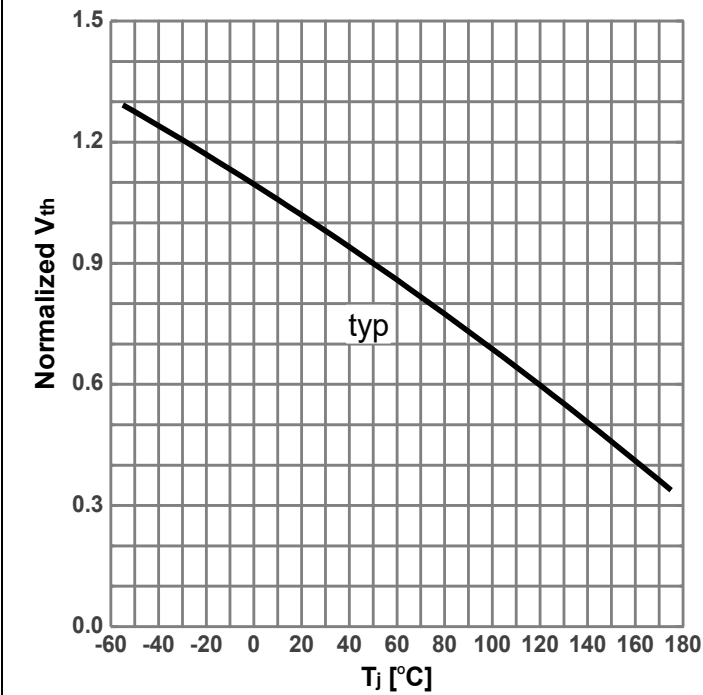

 $I_D = f(V_{DS}); T_J = 125^\circ\text{C}; \text{parameter: } V_{GS}$

Diagram 9: Typ. transfer characteristics



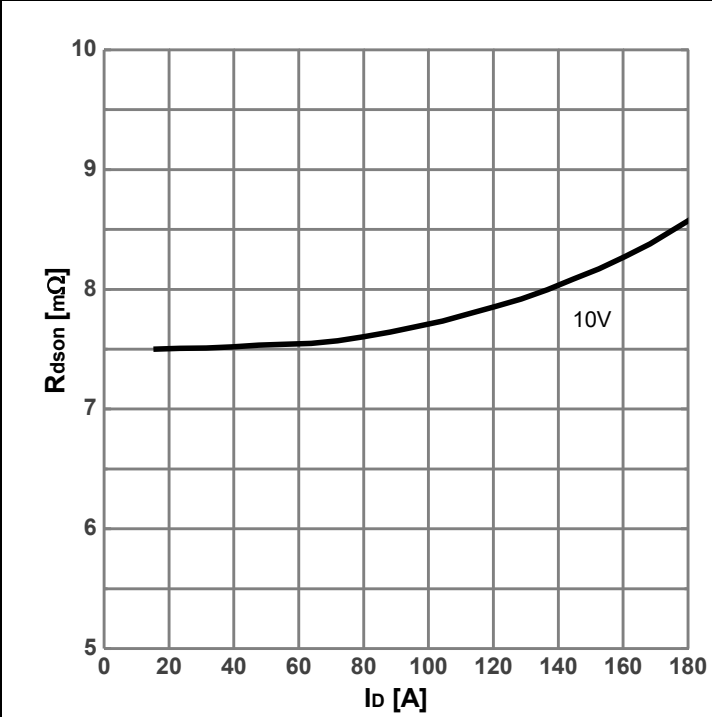
$I_D=f(V_{GS}); V_{DS}=15V; \text{parameter: } T_j$

Diagram 10: Gate threshold voltage vs. Junction temperature



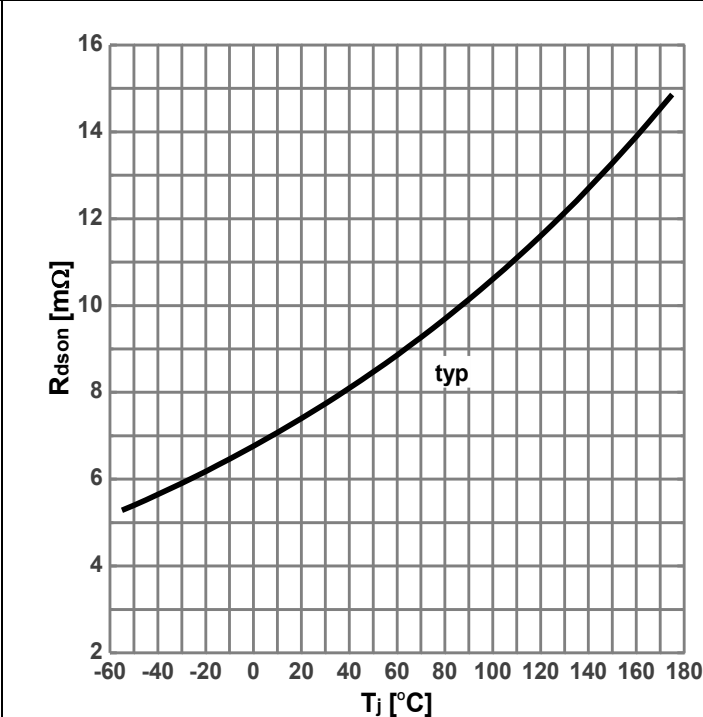
$V_{th}=f(T_j); I_D=250\mu A$

Diagram 11: On-state resistance vs. Drain current

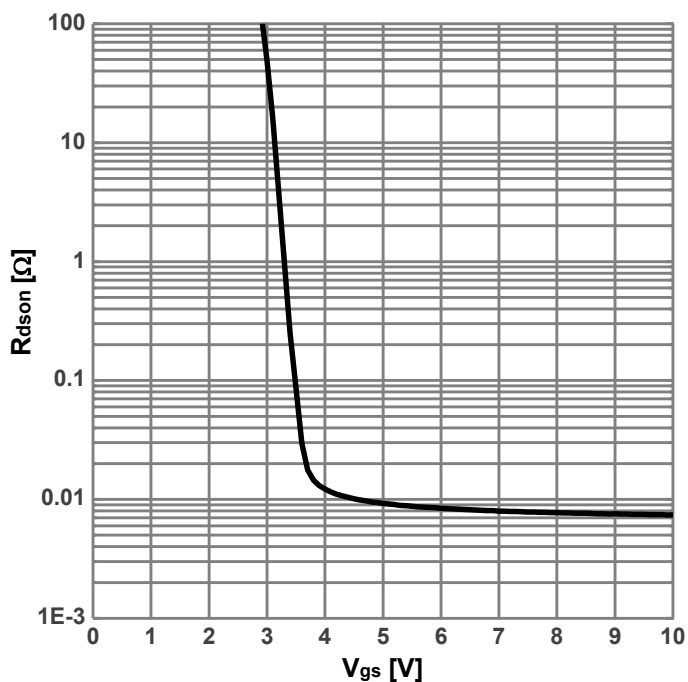


$R_{DS(on)}=f(I_D); T_j=25^{\circ}\text{C}; \text{parameter: } V_{GS}$

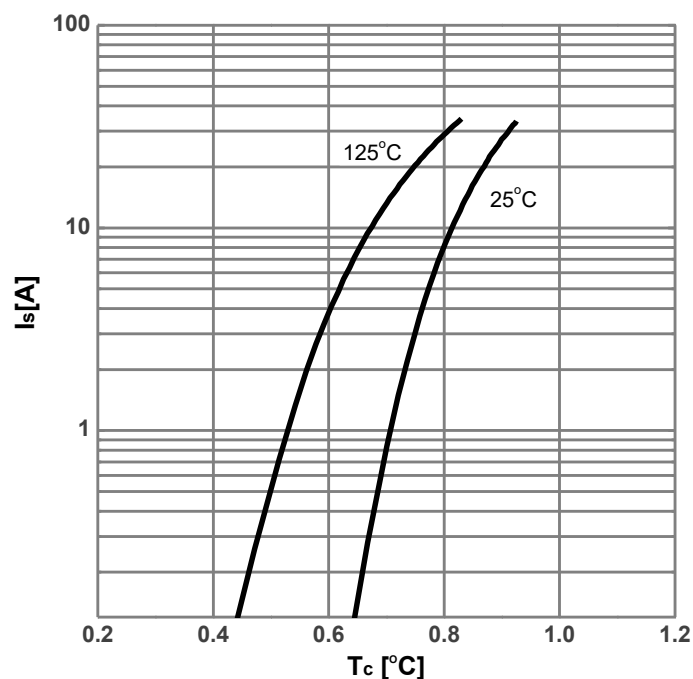
Diagram 12: On-state resistance vs. Junction temperature



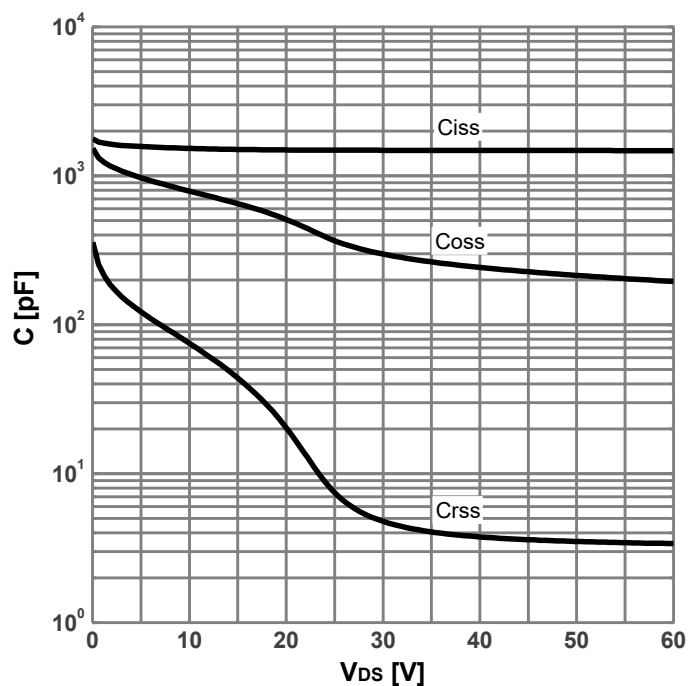
$R_{DS(on)}=f(T_j); I_D=20A; V_{GS}=10V$

Diagram 13: On-state resistance vs. V_{gs} characteristics

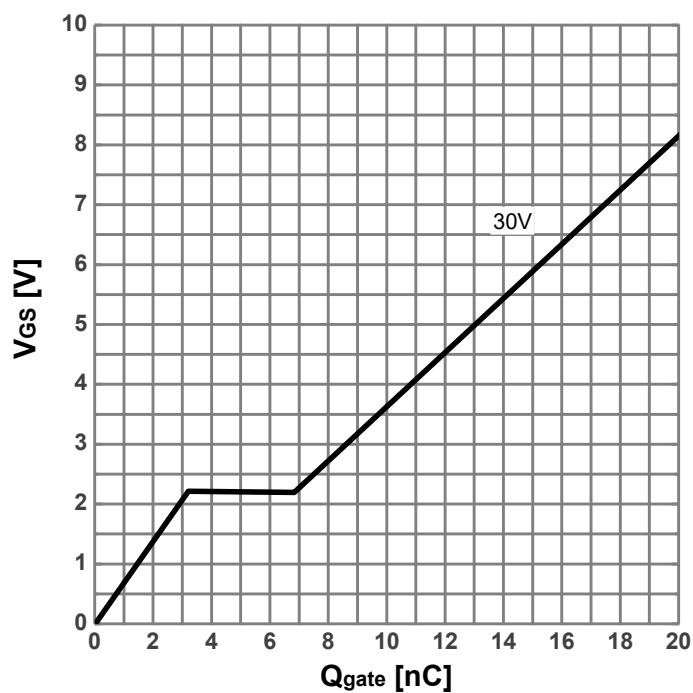
$$R_{DS(on)} = f(V_{GS}); T_J = 25^\circ\text{C}; I_D = 20\text{A}$$

Diagram 14: Forward characteristics of reverse diode

$$I_F = f(V_{SD}); \text{parameter: } T_J$$

Diagram 15: Typ. capacitances

$$C = f(V_{DS}); V_{GS} = 0\text{V}; f = 1\text{MHz}$$

Diagram 16: Typ. gate charge

$$V_{GS} = f(Q_{gate}); I_D = 14.5\text{A pulsed}; V_{DS} = 30\text{V}$$

6. Test Circuits

Table 7. Diode Characteristics

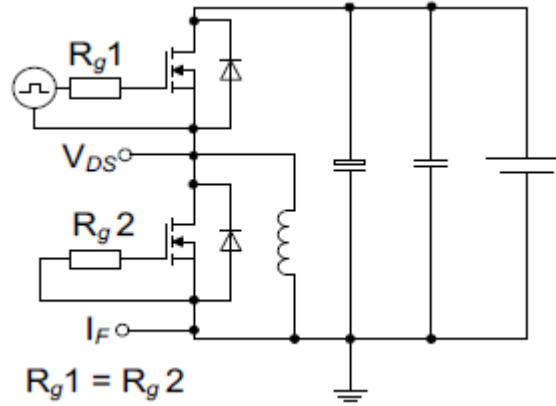
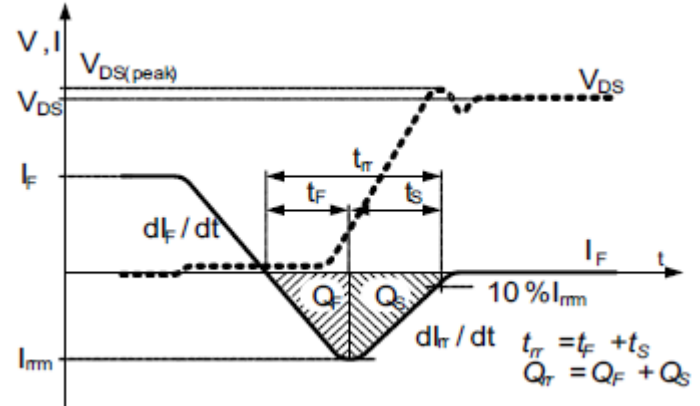
Test circuit for diode characteristics	Diode recovery waveform
	

Table 8. Switching Times

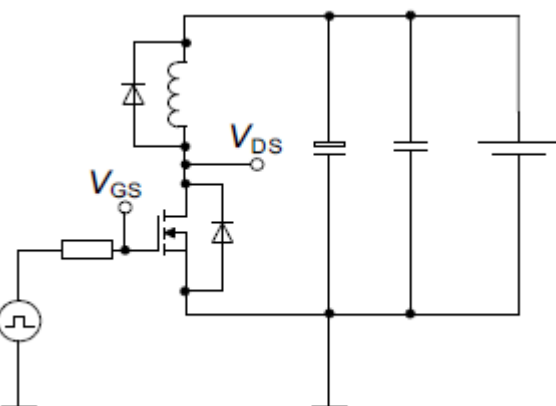
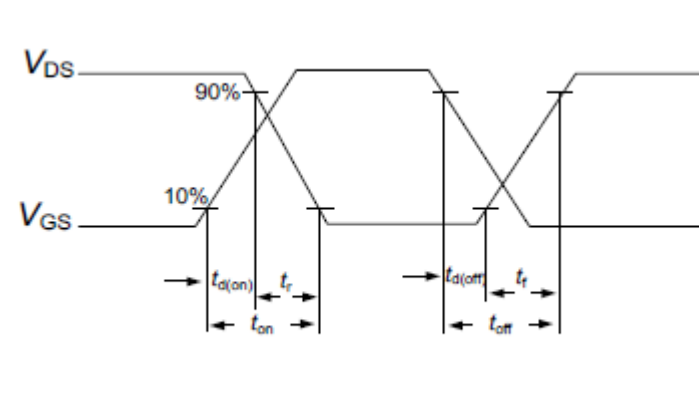
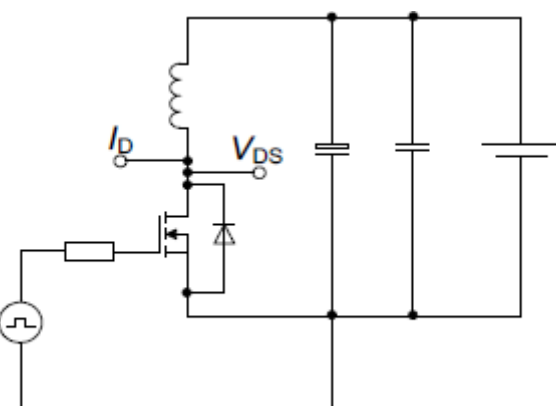
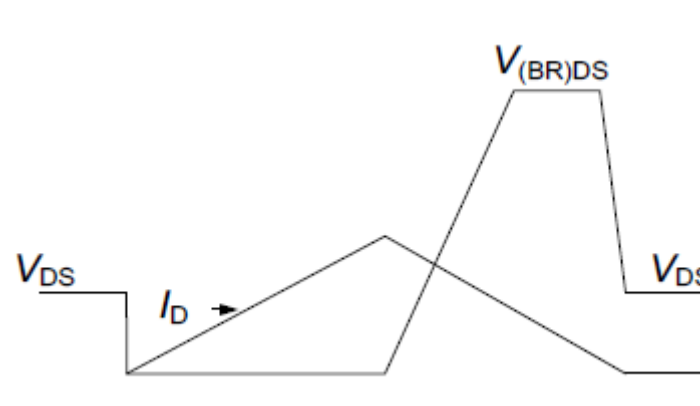
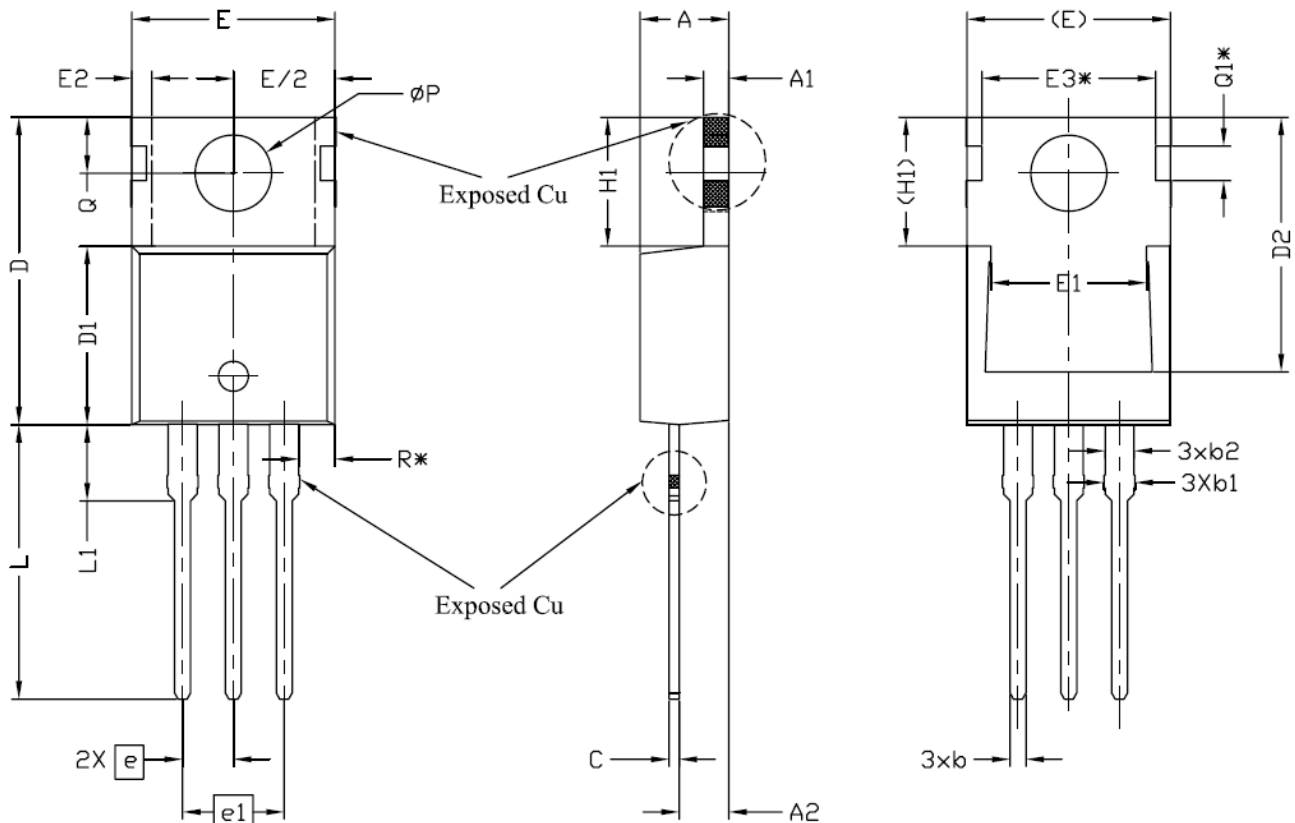
Switching times test circuit for inductive load	Switching times waveform
	

Table 9. Unclamped Inductive Load

Unclamped inductive load test circuit	Unclamped inductive waveform
	

7. Package Outlines

Figure 1 Outline TO-220 Dimensions in mm

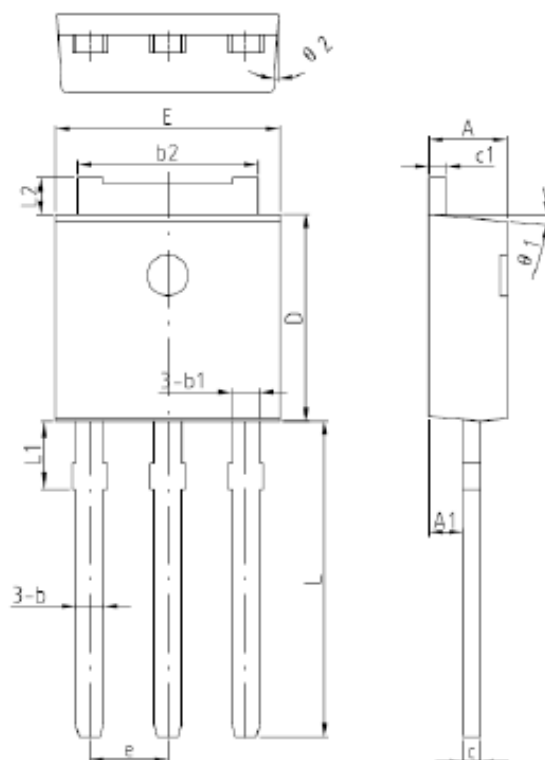


SYMBOL	DIMENSIONS			NOTES
	MIN.	NOM.	MAX.	
A	4.24	4.44	4.64	
A1	1.15	1.27	1.40	
A2	2.30	2.48	2.70	
b	0.70	0.80	0.90	
b1	1.20	1.55	1.75	
b2	1.20	1.45	1.70	
c	0.40	0.50	0.60	
D	14.70	15.37	16.00	4
D1	8.82	8.92	9.02	
D2	12.43	12.73	12.83	5
E	9.96	10.16	10.36	4,5
E1	6.86	7.77	8.89	5
E2	-	-	0.76	6
E3*	8.70REF.			
e	2.54BSC			
e1	5.08BSC			
H1	6.30	6.45	6.60	5,6
L	13.47	13.72	13.97	
L1	3.60	3.80	4.00	
ØP	3.75	3.84	3.93	
Q	2.60	2.80	3.00	
Q1*	1.73REF.			
R*	1.82REF.			

Note:

1. Package Reference: JEDEC TO220, Variation AB.
2. All Dimensions Are In mm.
3. Slot Required, Notch May Be Rounded
4. Dimension D & E Do Not Include Mold Flash. Mold Flash Shall Not Exceed 0.127mm Pre Side. These Dimensions Are Measured At The Outermost Extreme Of The Plastic Body.
5. Thermal Pad Contour Optional Within Dimensions E, H1, D2 & E1.
6. Dimension E2 & H1 Define A Zone Where Stamping And Singulation Irregularities Are Allowed.
7. "*" is reference .

Figure 2 Outline TO-251 Dimensions in mm



Symbol	Dimensions(mm)		
	Min.	Typ.	Max.
A	2.20	2.30	2.40
A1	0.90	1.01	1.17
b	0.50	-	0.91
b1	-	0.81	-
b2	5.13	5.33	5.46
c	0.46	0.50	0.60
c1	0.46	0.50	0.60
D	5.95	6.10	6.25
E	6.45	6.60	6.75
e	2.286(BSC)		
L	9.00	9.30	9.60
L1	-	2.00	-
L2	0.90	-	1.25
$\theta 1$	-	5°	-
$\theta 2$	-	3°	-

Figure 3 Outline TO-252 Dimensions in mm

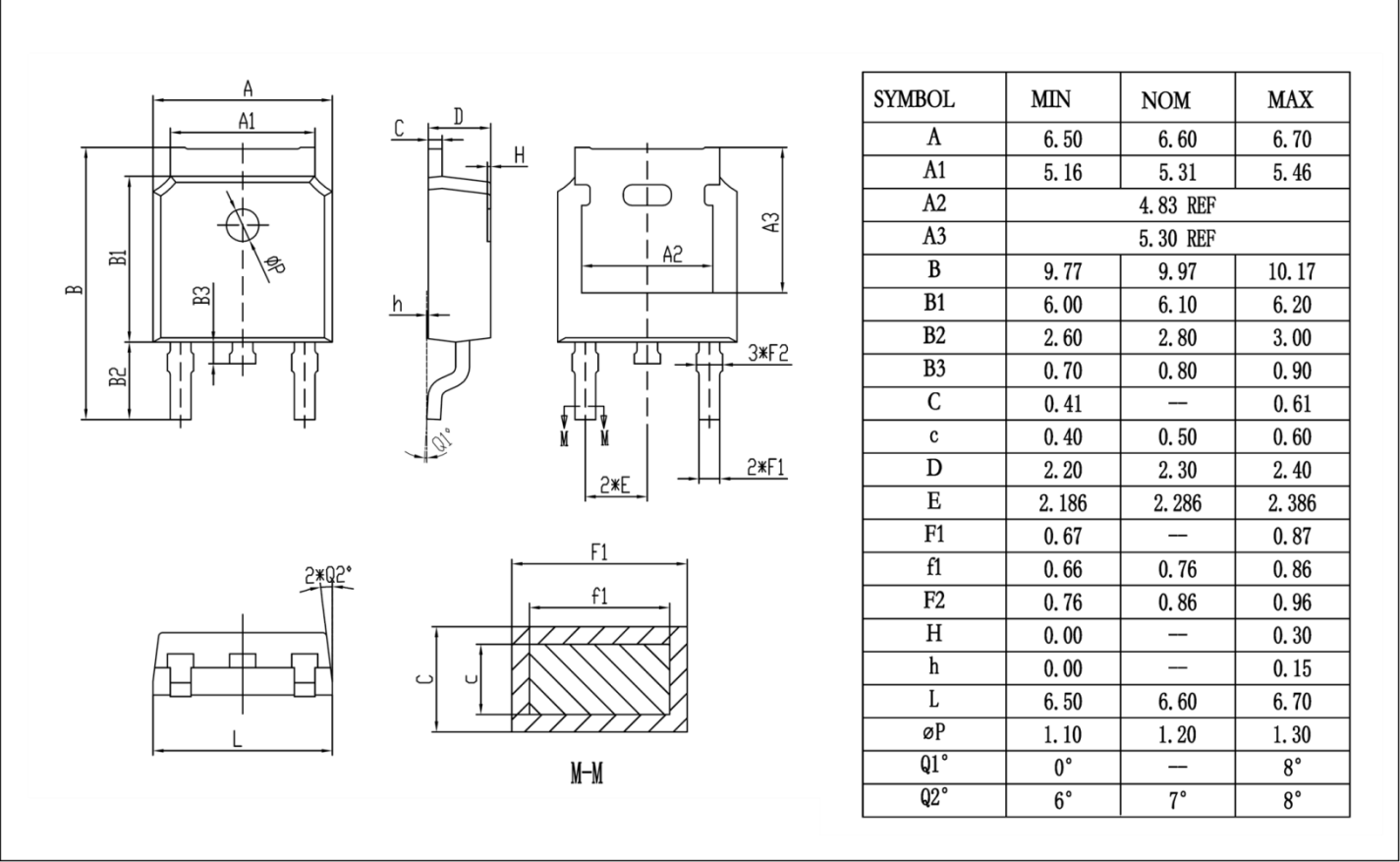
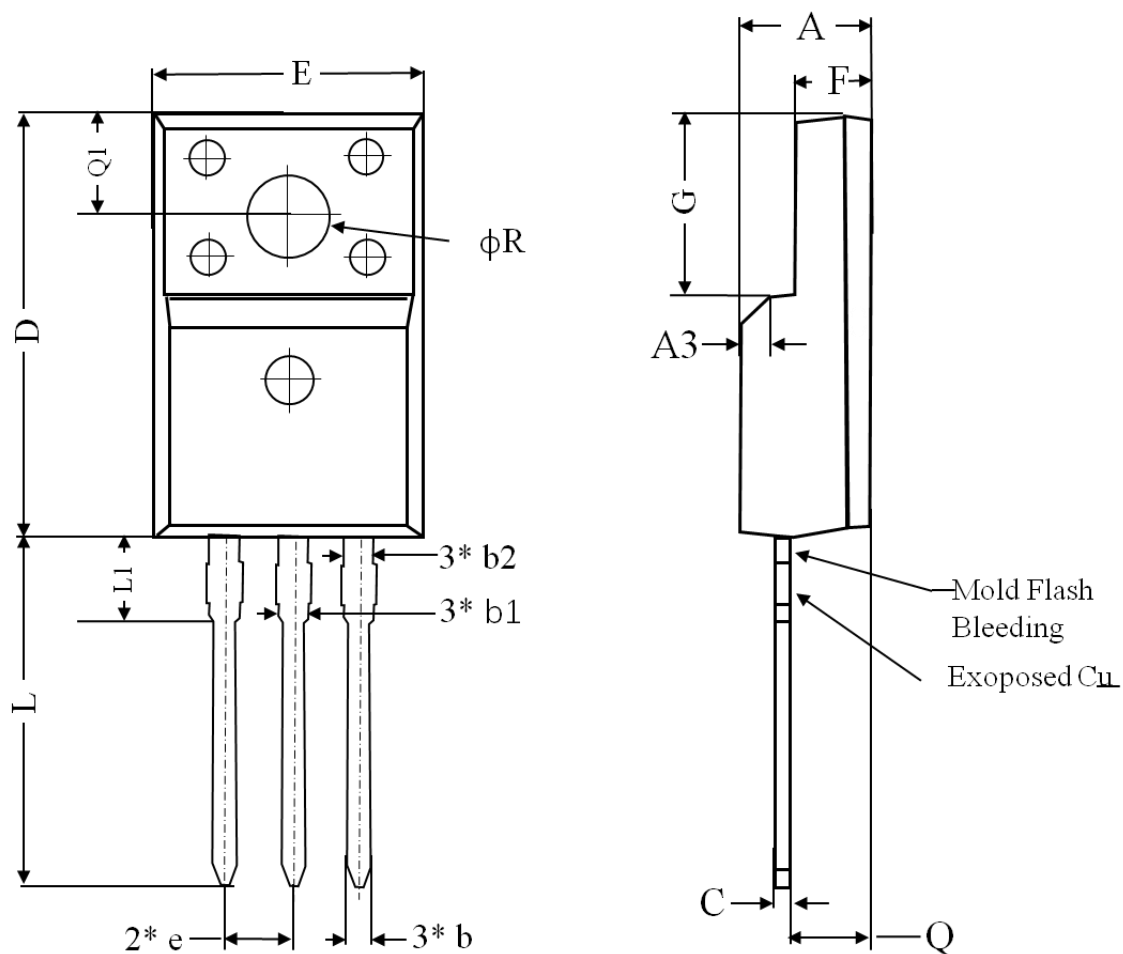


Figure 4 Outline TO-220 FullPAK Dimensions in mm



Note:

1. All Dimension Are In mm.
2. Package Body Sizes Exclude Mold Flash And Burrs Mold Flash Should Be less Than 6 Mil.

SYMBOL	DIMENSIONS		
	Min.	Nom.	Max.
A	4.60	4.70	4.80
b	0.70	0.80	0.91
b1	1.20	1.30	1.47
b2	1.10	1.20	1.30
C	0.45	0.50	0.63
D	15.80	15.87	15.97
e	2.54		
E	10.00	10.10	10.30
F	2.44	2.54	2.64
G	6.50	6.70	6.90
L	12.90	13.10	13.30
L1	3.13	3.23	3.33
Q	2.65	2.75	2.85
Q1	3.20	3.30	3.40
Φr	3.08	3.18	3.28

8. Appendix

CoolSemi Webpage: www.coolsemi.com.