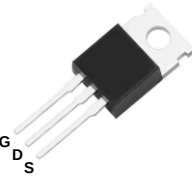
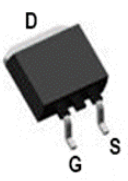
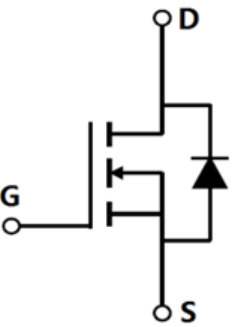


N-channel 150V, 6.6mΩ typ., 140A
SGT MOSFET S2 in TO-220 and TO-263

Datasheet - production data

1. Descriptions

TO-220	TO-263
	
Schematic Diagram	
	

Key Performance Parameters

Parameters	Value	Unit
BV_{DSS}	150	V
$R_{DS(on),max}$	7.5	mΩ
$Q_{g,typ}$	72	nC
$I_{D,pulse}$	500	A
E_{AS}	900	mJ

Features

- Extremely low losses due to very low FOM $R_{dson} \cdot Q_g$.
- High-speed switching.
- Qualified for industrial grade applications according to JEDEC.
- 100% UIS Tested.

Applications

High-Efficiency DC-DC Converters, Switching Voltage Regulators and Motor Drivers.

Type/Ordering Code	Package	Marking	Related Links
CSP075N15S2A	TO-220	075N15S2A	See Appendix A
CSB075N15S2A	TO-263		

Contents

1.	Descriptions	1
2.	Maximum Ratings.....	3
3.	Thermal Characteristics	4
4.	Electrical Characteristics	5
5.	Electrical Characteristics Diagrams	6
6.	Test Circuits	10
7.	Package Outlines	11
8.	Appendix.....	13

2. Maximum Ratings

at $T_j = 25^\circ\text{C}$, unless otherwise specified

Table 1. Absolute Maximum Ratings

Symbol	Parameter	Values			Unit	Test Condition
		Min.	Typ.	Max.		
V_{DS}	Drain-source voltage ¹⁾	-	-	150	V	$V_{GS}=0V$, $I_D=250\mu A$
I_D	Continuous drain current (Silicon Limited) ²⁾	-	-	140	A	$T_C=25^\circ\text{C}$
$I_{D,pulse}$	Pulsed drain current	-	-	500	A	$T_C=25^\circ\text{C}$
E_{AS}	Avalanche energy, single pulse ³⁾	-	-	900	mJ	$I_D=60A$; $V_{DD}=50V$
I_{AS}	Avalanche current	-	-	60	A	-
V_{GS}	Gate source voltage	-20	-	20	V	static; AC ($f>1\text{ Hz}$)
P_{tot}	Power dissipation	-	-	300	W	$T_C=25^\circ\text{C}$
T_j, T_{stg}	Operating and storage temperature	-55	-	175	$^\circ\text{C}$	-
I_S	Continuous diode forward current	-	-	140	A	$T_C=25^\circ\text{C}$
$I_{S,pulse}$	Diode pulse current ²⁾	-	-	500	A	$T_C=25^\circ\text{C}$

1) Limited by T_j max. Maximum duty cycle $D=0.75$.

2) Pulse width t_p limited by $T_{j,max}$.

3) $V_{DD}=50V$, $L=0.5mH$, $R_G=25\Omega$, Starting $T_j=25^\circ\text{C}$.

3. Thermal Characteristics

Table 2. Thermal Characteristics

Symbol	Parameter	Values			Unit	Test Condition
		Min.	Typ.	Max.		
R_{thJC}	Thermal resistance, junction - case	-	-	0.5	°C/W	$T_C = 25^{\circ}\text{C}$
R_{thJA}	Thermal resistance, junction - ambient	-	-	60	°C/W	$T_C = 25^{\circ}\text{C}$
T_{sold}	Soldering temperature, wavesoldering only allowed at leads	-	-	260	°C	Lead Temperature (Soldering, 10 sec)

4. Electrical Characteristics

at $T_j = 25^\circ\text{C}$, unless otherwise specified

Table 3. Static Characteristics

Symbol	Parameter	Values			Unit	Test Condition
		Min.	Typ.	Max.		
$V_{(BR)DSS}$	Drain-source breakdown voltage	150	-	-	V	$V_{GS}=0V, I_D=250\mu A$
$V_{(GS)th}$	Gate threshold voltage	2	3.0	4	V	$V_{DS}=V_{GS}, I_D=250\mu A$
I_{DSS}	Zero gate voltage drain current	-	-	1	μA	$V_{DS}=150V, V_{GS}=0V, T_j=25^\circ C$
I_{GSS}	Gate-source leakage current	-	-	± 100	nA	$V_{GS}=\pm 20V, V_{DS}=0V$
$R_{DS(on)}$	Drain-source on-state resistance	-	6.6	7.5	m Ω	$V_{GS}=10V, I_D=20A, T_j=25^\circ C$
R_G	Gate resistance	-	2.4	-	Ω	$V_{DD}=0V, V_{GS}=0V, F=1MHz$
g_{fs}	Transconductance		80		S	$V_{DS}=5V, I_D=20A$

Table 4. Dynamic Characteristics

Symbol	Parameter	Values			Unit	Test Condition
		Min.	Typ.	Max.		
C_{iss}	Input capacitance	-	5240	-	pF	$V_{GS}=0V, V_{DS}=75V, f=1MHz$
C_{oss}	Output capacitance	-	412	-	pF	$V_{GS}=0V, V_{DS}=75V, f=1MHz$
C_{rss}	Reverse transfer capacitance	-	10	-	pF	$V_{GS}=0V, V_{DS}=75V, f=1MHz$
$t_{d(on)}$	Turn-on delay time	-	22	-	ns	$V_{DD}=75V, V_{GS}=10V, I_D=100A, R_G=1.6\Omega$
t_r	Rise time	-	115	-	ns	$V_{DD}=75V, V_{GS}=10V, I_D=100A, R_G=1.6\Omega$
$t_{d(off)}$	Turn-off delay time	-	44	-	ns	$V_{DD}=75V, V_{GS}=10V, I_D=100A, R_G=1.6\Omega$
t_f	Fall time	-	105	-	ns	$V_{DD}=75V, V_{GS}=10V, I_D=100A, R_G=1.6\Omega$

Table 5. Gate Charge Characteristics

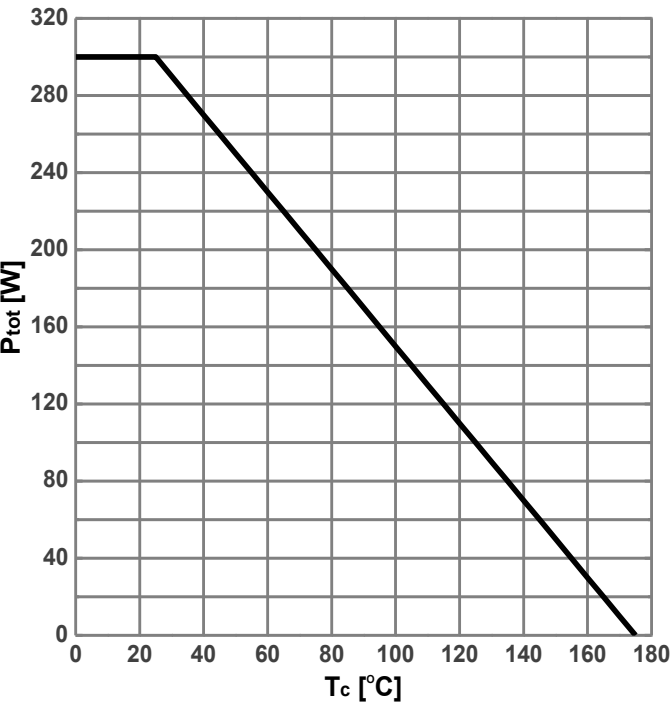
Symbol	Parameter	Values			Unit	Test Condition
		Min.	Typ.	Max.		
Q_{gs}	Gate to source charge	-	18	-	nC	$V_{DD}=75V, I_D=20A, V_{GS}=0 \text{ to } 10V$
Q_{gd}	Gate to drain charge	-	10	-	nC	$V_{DD}=75V, I_D=20A, V_{GS}=0 \text{ to } 10V$
Q_g	Gate charge total	-	72	-	nC	$V_{DD}=75V, I_D=20A, V_{GS}=0 \text{ to } 10V$
$V_{plateau}$	Gate plateau voltage	-	3.4	-	V	$V_{DD}=75V, I_D=20A, V_{GS}=0 \text{ to } 10V$

Table 6. Reverse Diode Characteristics

Symbol	Parameter	Values			Unit	Test Condition
		Min.	Typ.	Max.		
V_{SD}	Diode forward voltage	-	0.76	-	V	$V_{GS}=0V, I_F=10A, T_j=25^\circ C$
t_{rr}	Reverse recovery time	-	45	-	ns	$V_R=75V, I_F=100A, di_F/dt=100A/\mu s$
Q_{rr}	Reverse recovery charge	-	12	-	nC	$V_R=75V, I_F=100A, di_F/dt=100A/\mu s$
I_{rrm}	Peak reverse recovery current	-	1.2	-	A	$V_R=75V, I_F=100A, di_F/dt=100A/\mu s$

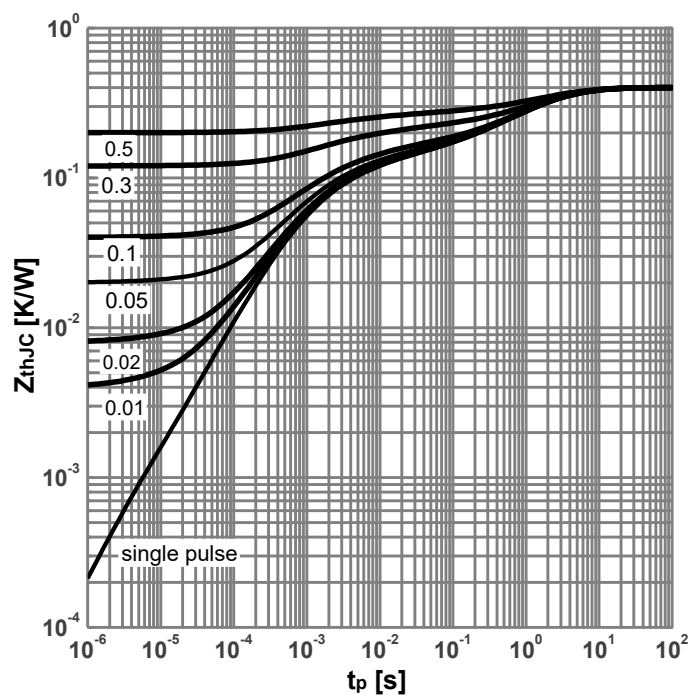
5. Electrical Characteristics Diagrams

Diagram 1: Power dissipation



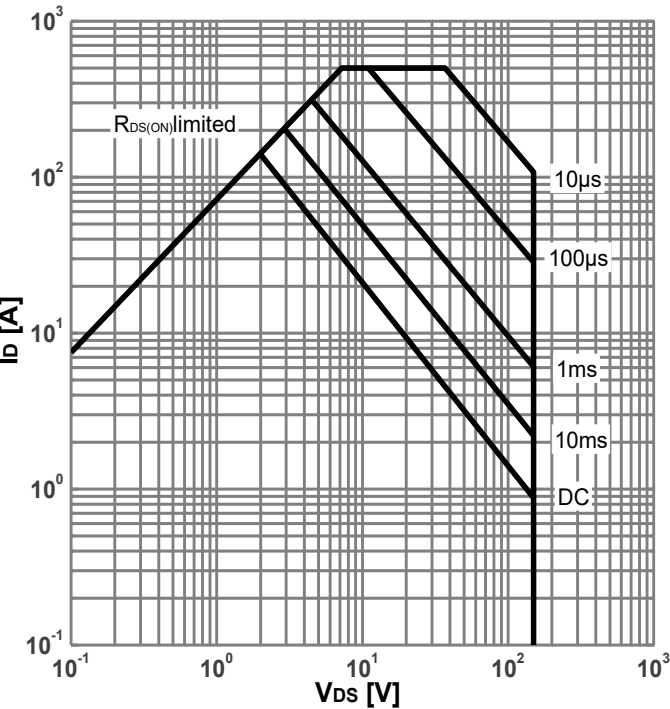
$P_{tot}=f(T_c)$

Diagram 2: Max. transient thermal impedance



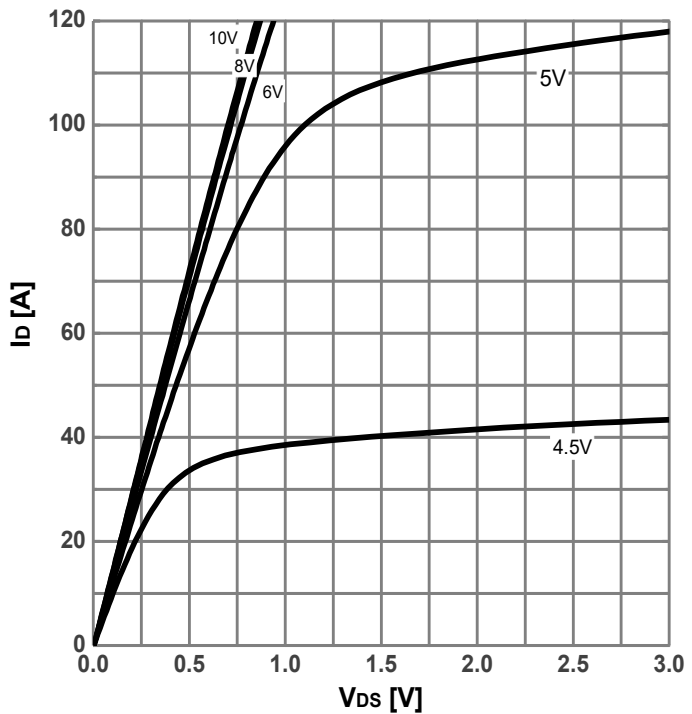
$Z_{thJC}=f(t_p)$; parameter: $D= t_p/T$

Diagram 3: Safe operating area



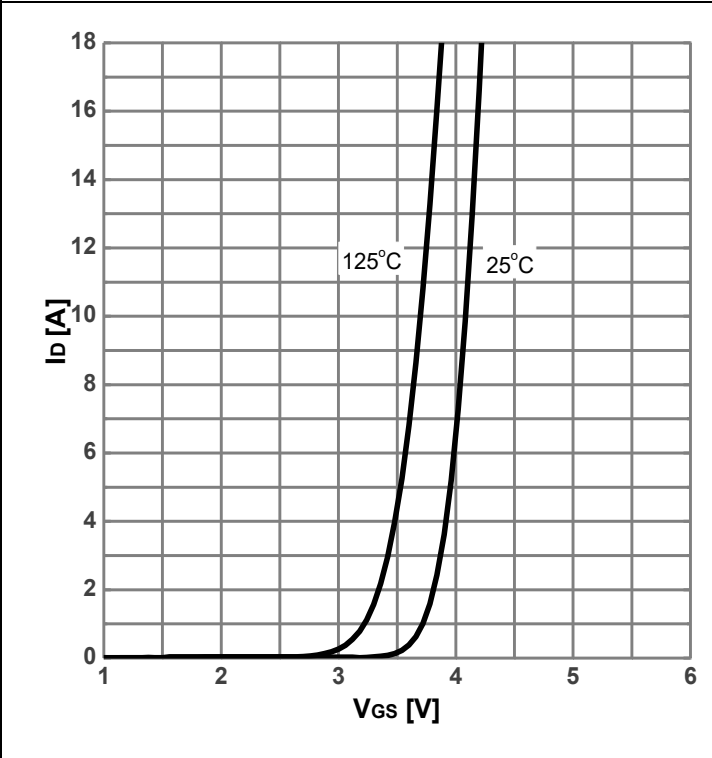
$I_D=f(V_{DS})$; $T_J=25^{\circ}C$; $D=0$; parameter: t_p

Diagram 4: Typ. output characteristics



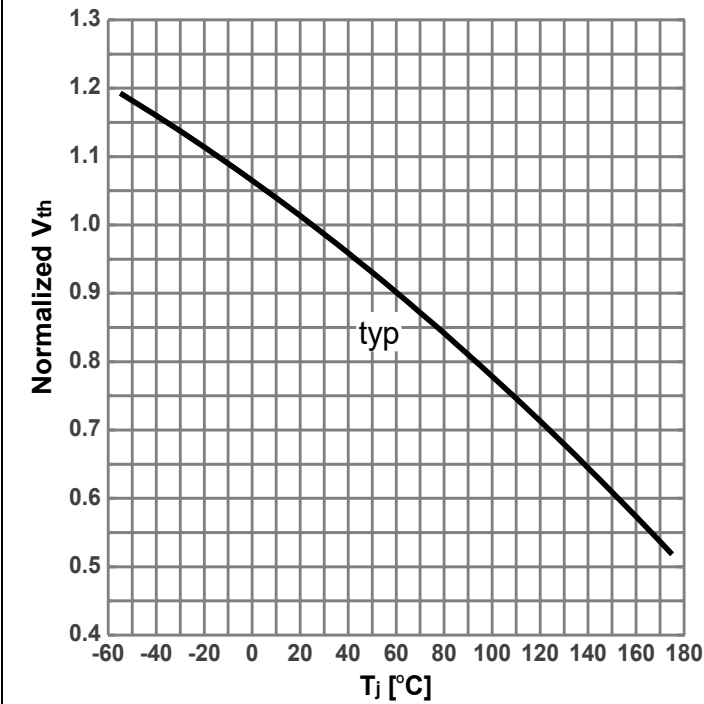
$I_D=f(V_{DS})$; $T_J=25^{\circ}C$; parameter: V_{GS}

Diagram 5: Typ. transfer characteristics



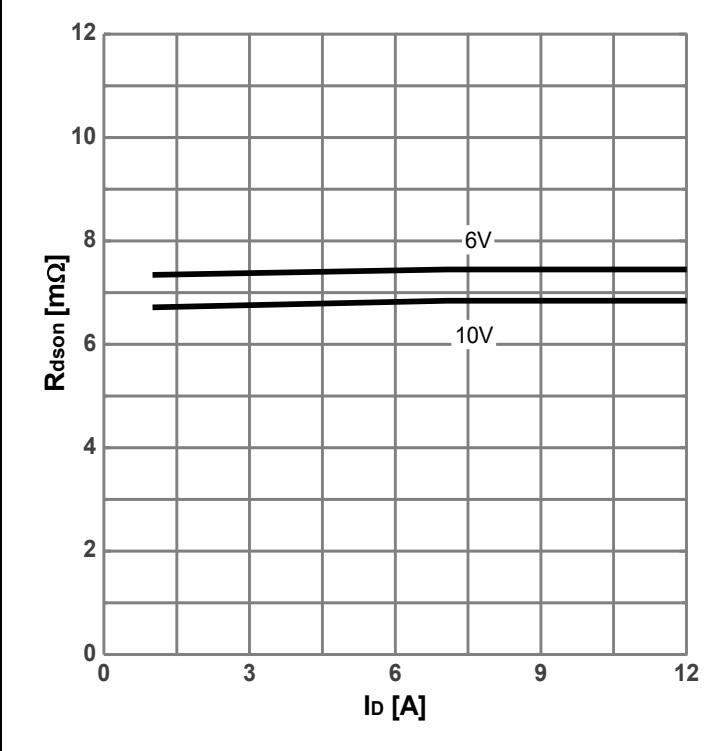
$I_D=f(V_{GS}); V_{DS}=5V; \text{parameter: } T_j$

Diagram 6: Gate threshold voltage vs. Junction temperature



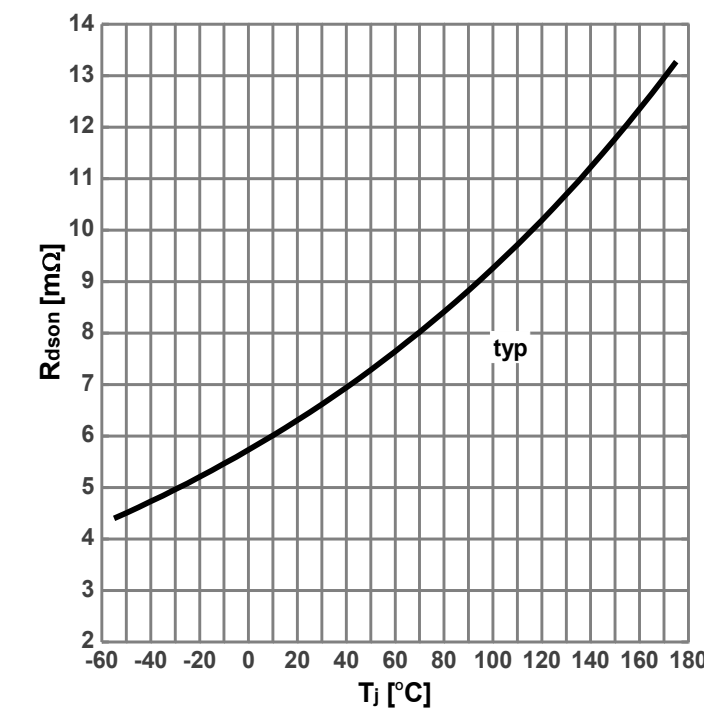
$V_{th}=f(T_j); I_D=250\mu A$

Diagram 7: On-state resistance vs. Drain current



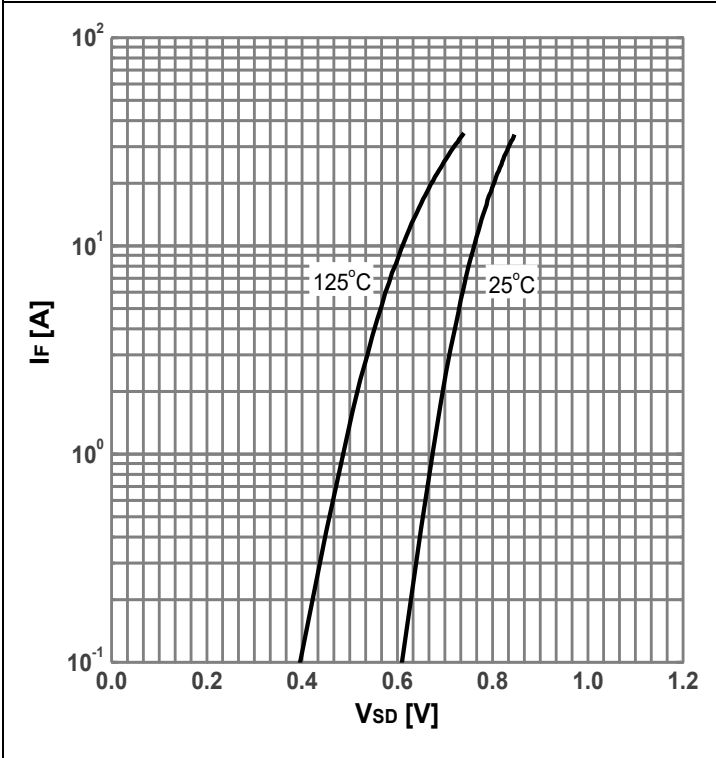
$R_{DS(on)}=f(I_D); T_j=25^{\circ}\text{C}; \text{parameter: } V_{GS}$

Diagram 8: On-state resistance vs. Junction temperature



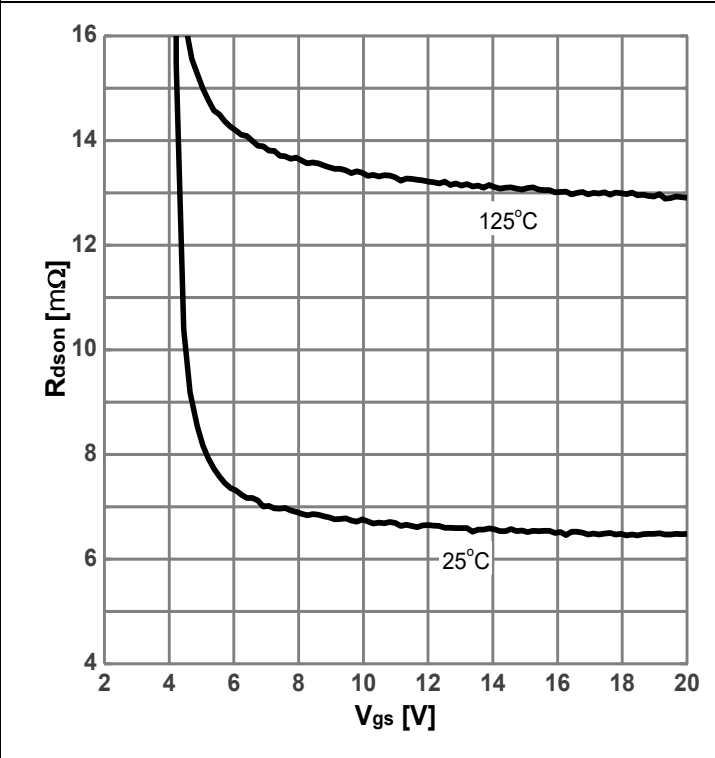
$R_{DS(on)}=f(T_j); I_D=20A; V_{GS}=10V$

Diagram 9: Forward characteristics of reverse diode



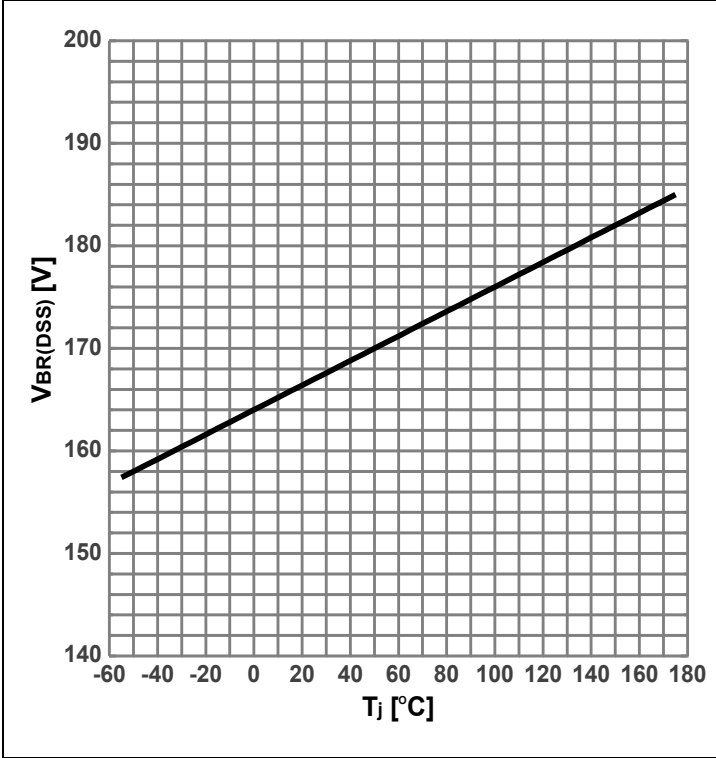
$I_F=f(V_{SD})$; parameter: T_j

Diagram 10: On-state resistance vs. V_{GS} characteristics



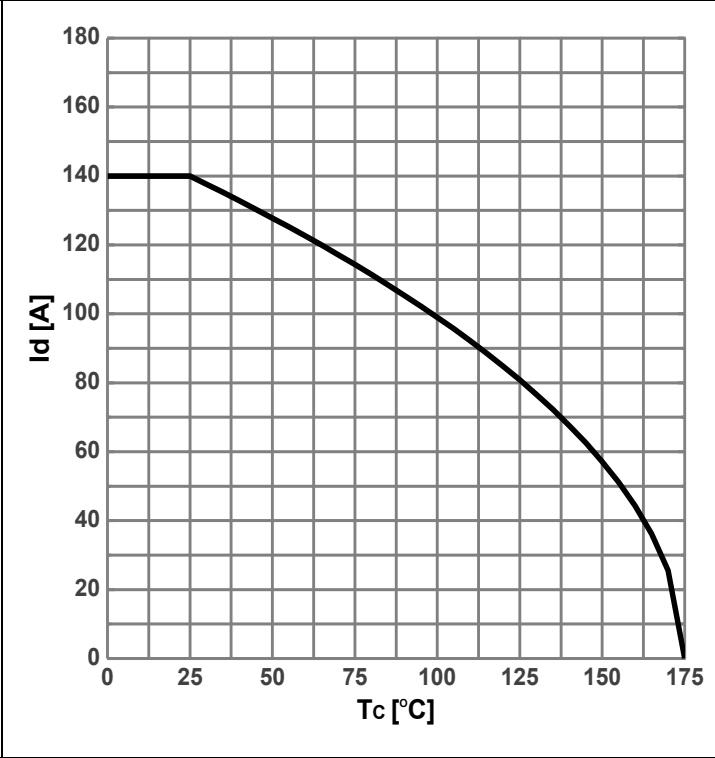
$R_{DS(on)}=f(V_{GS})$; $I_D=20A$; parameter: T_j

Diagram 11: Breakdown Voltage Variation vs. Temperature



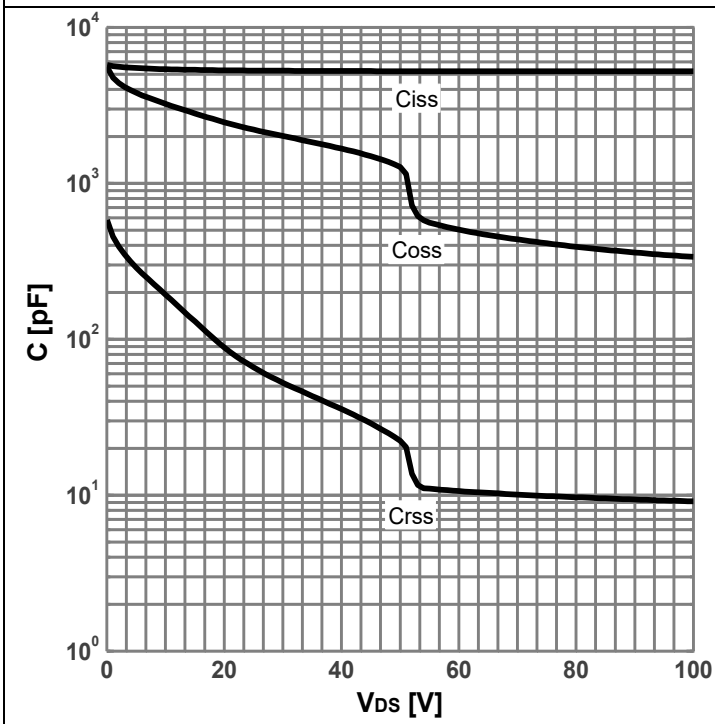
$V_{BR(DSS)}=f(T_j)$; $I_D=250\mu A$

Diagram 12: Maximum Drain Current



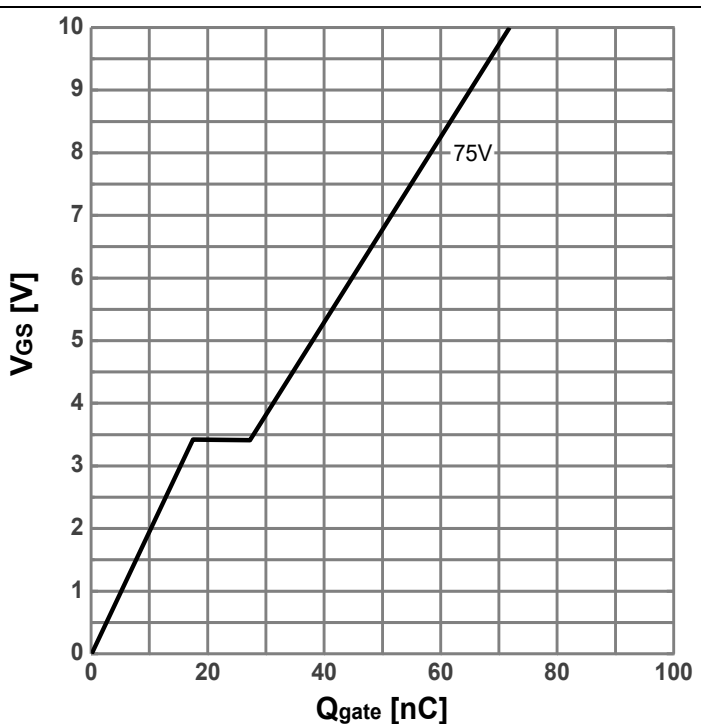
$I_D=f(T_c)$; $V_{GS}=10V$

Diagram 13: Typ. capacitances



$C=f(V_{DS}); V_{GS}=0V; f=1MHz$

Diagram 14: Typ. gate charge



$V_{GS}=f(Q_{gate}); I_D=20A$ pulsed; $V_{DS}=75V$

6. Test Circuits

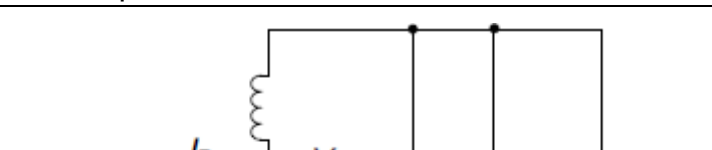
Table 7. Diode Characteristics

Test circuit for diode characteristics $R_{g1} = R_{g2}$	Diode recovery waveform $t_{TR} = t_F + t_S$ $Q_{TR} = Q_F + Q_S$
---	---

Table 8. Switching Times

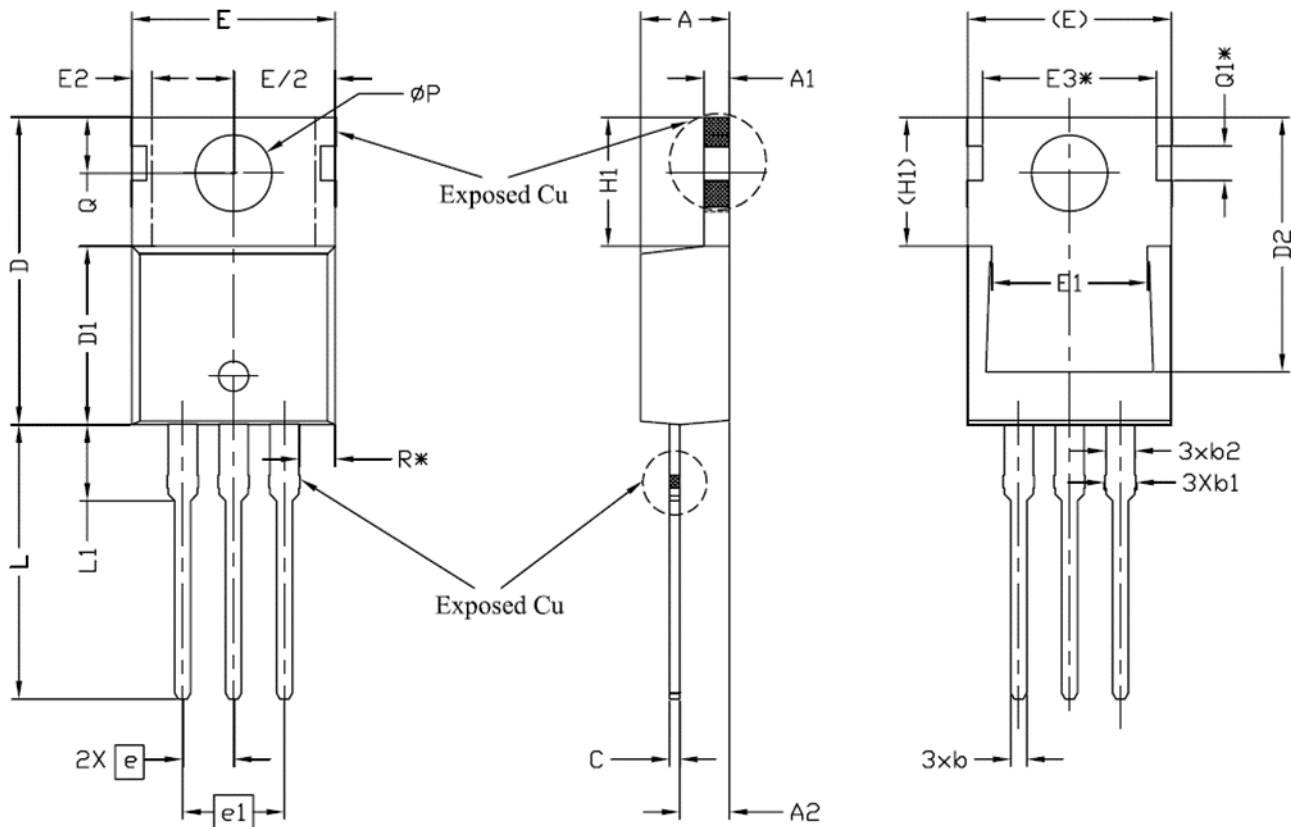
Switching times test circuit for inductive load	Switching times waveform

Table 9. Unclamped Inductive Load

Unclamped inductive load test circuit 	Unclamped inductive waveform 
---	--

7. Package Outlines

Figure 1 Outline TO-220 Dimensions in mm



SYMBOL	DIMENSIONS			NOTES
	MIN.	NOM.	MAX.	
A	4.24	4.44	4.64	
A1	1.15	1.27	1.40	
A2	2.30	2.48	2.70	
b	0.70	0.80	0.90	
b1	1.20	1.55	1.75	
b2	1.20	1.45	1.70	
c	0.40	0.50	0.60	
D	14.70	15.37	16.00	4
D1	8.82	8.92	9.02	
D2	12.43	12.73	12.83	5
E	9.96	10.16	10.36	4,5
E1	6.86	7.77	8.89	5
E2	-	-	0.76	6
E3*	8.70REF.			
e	2.54BSC			
e1	5.08BSC			
H1	6.30	6.45	6.60	5,6
L	13.47	13.72	13.97	
L1	3.60	3.80	4.00	
øP	3.75	3.84	3.93	
Q	2.60	2.80	3.00	
Q1*	1.73REF.			
R*	1.82REF.			

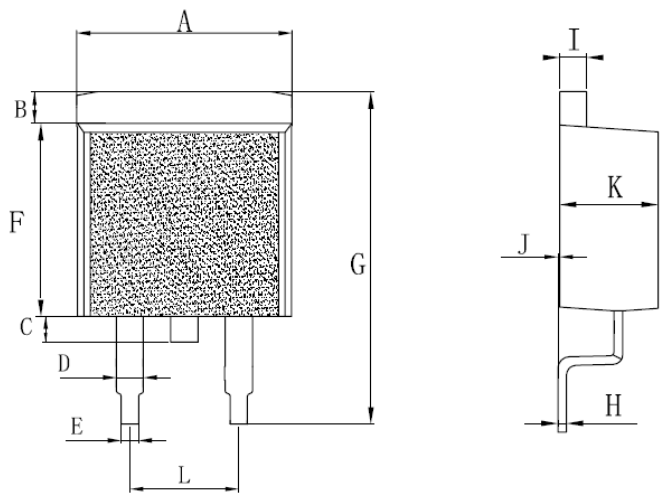
Note:

1. Package Reference: JEDEC TO220, Variation AB.
2. All Dimensions Are In mm.
3. Slot Required, Notch May Be Rounded
4. Dimension D & E Do Not Include Mold Flash. Mold Flash Shall Not Exceed 0.127mm Pre Side. These Dimensions Are Measured At The Outermost Extreme Of The Plastic Body.
5. Thermal Pad Contour Optional Within Dimensions E, H1, D2 & E1.
6. Dimension E2 & H1 Define A Zone Where Stamping And Singulation Irregularities Are Allowed.
7. "*" is reference .

Figure 2 Outline TO-263 Dimensions in mm

PACKAGE OUTLINE DIMENSIONS

TO-263



DIM.	Unit(mm)		Unit(inch)	
	Min	Max	Min	Max
A	9.7	10.4	0.381	0.409
B	1.31	1.62	0.051	0.063
C	0.65	1.22	0.025	0.048
D	1.15	1.36	0.045	0.053
E	0.62	0.95	0.024	0.037
F	8.75	9.32	0.344	0.366
G	14.75	15.8	0.580	0.622
H	0.32	0.48	0.012	0.018
I	1.18	1.36	0.046	0.053
J	0	0.15	0	0.005
K	4.38	4.86	0.172	0.191
L	4.85	5.23	0.190	0.205

8. Appendix

CoolSemi Webpage: www.coolsemi.com.