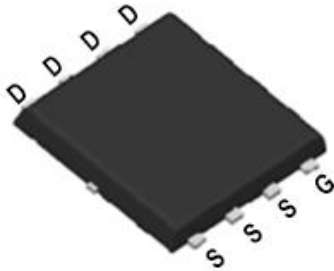
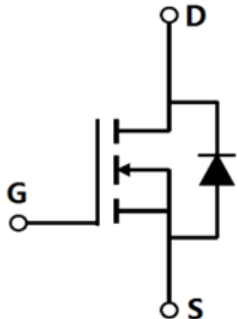


N-channel 80V, 9.5mΩ typ., 68A
 SGT MOSFET S2 in DFN5*6

Datasheet - production data

1. Descriptions

DFN5*6

Schematic Diagram


Key Performance Parameters

Parameters	Value	Unit
BV_{DSS}	80	V
$R_{DS(on),max}$	12	mΩ
$Q_{g,typ}$	26	nC
$I_{D,pulse}$	148	A
E_{AS}	180	mJ

Features

- Extremely low losses due to very low FOM $R_{dson} \cdot Q_g$.
- High-speed switching.
- Qualified for industrial grade applications according to JEDEC.
- 100% UIS Tested.

Applications

High-Efficiency DC-DC Converters, Switching Voltage Regulators and Motor Drivers.

Type/Ordering Code	Package	Marking	Related Links
CSLS120N08S2	DFN5*6	120N08S2	See Appendix A

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2. Maximum Ratings

at $T_j = 25^\circ\text{C}$, unless otherwise specified

Table 1. Absolute Maximum Ratings

Symbol	Parameter	Values			Unit	Test Condition
		Min.	Typ.	Max.		
V_{DS}	Drain-source voltage ¹⁾	-	-	80	V	$V_{GS}=0V$, $I_D=250\mu A$
I_D	Continuous drain current (Silicon Limited)	-	-	68	A	$T_C=25^\circ\text{C}$
$I_{D,pulse}$	Pulsed drain current	-	-	148	A	$T_C=25^\circ\text{C}$
E_{AS}	Avalanche energy, single pulse ²⁾	-	-	180	mJ	$I_D=30A$; $V_{DD}=50V$
I_{AS}	Avalanche current	-	-	30	A	-
V_{GS}	Gate source voltage	-20	-	20	V	static; AC ($f>1\text{ Hz}$)
P_{tot}	Power dissipation	-	-	75	W	$T_C=25^\circ\text{C}$
T_j, T_{stg}	Operating and storage temperature	-55	-	150	$^\circ\text{C}$	-
I_S	Continuous diode forward current	-	-	68	A	$T_C=25^\circ\text{C}$
$I_{S,pulse}$	Diode pulse current ²⁾	-	-	148	A	$T_C=25^\circ\text{C}$

1) Limited by T_j max. Maximum duty cycle $D=0.75$.

2) Pulse width t_p limited by $T_{j,max}$.

3) $V_{DD}=50V$, $L=0.4mH$, $R_G=25\Omega$, Starting $T_j=25^\circ\text{C}$.

3. Thermal Characteristics

Table 2. Thermal Characteristics

Symbol	Parameter	Values			Unit	Test Condition
		Min.	Typ.	Max.		
R_{thJC}	Thermal resistance, junction - case	-	-	2	°C/W	$T_C = 25^{\circ}\text{C}$
R_{thJA}	Thermal resistance, junction - ambient	-	-	62	°C/W	$T_C = 25^{\circ}\text{C}$
T_{sold}	Soldering temperature, wavesoldering only allowed at leads	-	-	260	°C	Lead Temperature (Soldering, 10 sec)

4. Electrical Characteristics

at $T_j = 25^\circ\text{C}$, unless otherwise specified

Table 3. Static Characteristics

Symbol	Parameter	Values			Unit	Test Condition
		Min.	Typ.	Max.		
$V_{(BR)DSS}$	Drain-source breakdown voltage	80	-	-	V	$V_{GS}=0V, I_D=250\mu A$
$V_{(GS)th}$	Gate threshold voltage	1.0	1.8	2.5	V	$V_{DS}=V_{GS}, I_D=250\mu A$
I_{DSS}	Zero gate voltage drain current	-	-	1	μA	$V_{DS}=80V, V_{GS}=0V, T_j=25^\circ C$
I_{GSS}	Gate-source leakage current	-	-	± 100	nA	$V_{GS}=\pm 20V, V_{DS}=0V$
$R_{DS(on)}$	Drain-source on-state resistance	-	9.5	12	m Ω	$V_{GS}=10V, I_D=15A, T_j=25^\circ C$
R_G	Gate resistance	-	1.9	-	Ω	$V_{DD}=0V, V_{GS}=0V, F=1MHz$
g_{fs}	Transconductance		40		S	$V_{DS}=5V, I_D=15A$

Table 4. Dynamic Characteristics

Symbol	Parameter	Values			Unit	Test Condition
		Min.	Typ.	Max.		
C_{iss}	Input capacitance	-	1450	-	pF	$V_{GS}=0V, V_{DS}=40V, f=1MHz$
C_{oss}	Output capacitance	-	209	-	pF	$V_{GS}=0V, V_{DS}=40V, f=1MHz$
C_{rss}	Reverse transfer capacitance	-	4.0	-	pF	$V_{GS}=0V, V_{DS}=40V, f=1MHz$
$t_{d(on)}$	Turn-on delay time	-	19	-	ns	$V_{DD}=40V, V_{GS}=10V, I_D=14.5A, R_G=3\Omega$
t_r	Rise time	-	10	-	ns	$V_{DD}=40V, V_{GS}=10V, I_D=14.5A, R_G=3\Omega$
$t_{d(off)}$	Turn-off delay time	-	24.6	-	ns	$V_{DD}=40V, V_{GS}=10V, I_D=14.5A, R_G=3\Omega$
t_f	Fall time	-	5	-	ns	$V_{DD}=40V, V_{GS}=10V, I_D=14.5A, R_G=3\Omega$

Table 5. Gate Charge Characteristics

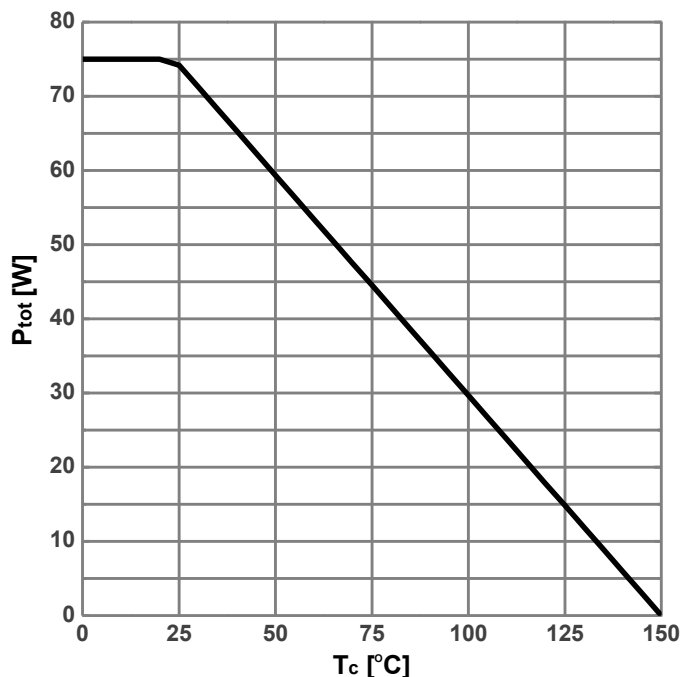
Symbol	Parameter	Values			Unit	Test Condition
		Min.	Typ.	Max.		
Q_{gs}	Gate to source charge	-	6.4	-	nC	$V_{DD}=40V, I_D=14.5A, V_{GS}=0 \text{ to } 10V$
Q_{gd}	Gate to drain charge	-	3.2	-	nC	$V_{DD}=40V, I_D=14.5A, V_{GS}=0 \text{ to } 10V$
Q_g	Gate charge total	-	26	-	nC	$V_{DD}=40V, I_D=14.5A, V_{GS}=0 \text{ to } 10V$
$V_{plateau}$	Gate plateau voltage	-	3.1	-	V	$V_{DD}=40V, I_D=14.5A, V_{GS}=0 \text{ to } 10V$

Table 6. Reverse Diode Characteristics

Symbol	Parameter	Values			Unit	Test Condition
		Min.	Typ.	Max.		
V_{SD}	Diode forward voltage	-	0.82	-	V	$V_{GS}=0V, I_F=15A, T_j=25^\circ C$
t_{rr}	Reverse recovery time	-	17	-	ns	$V_R=40V, I_F=10A, di_F/dt=100A/\mu s$
Q_{rr}	Reverse recovery charge	-	64	-	μC	$V_R=40V, I_F=10A, di_F/dt=100A/\mu s$
I_{rrm}	Peak reverse recovery current	-	19	-	A	$V_R=40V, I_F=10A, di_F/dt=100A/\mu s$

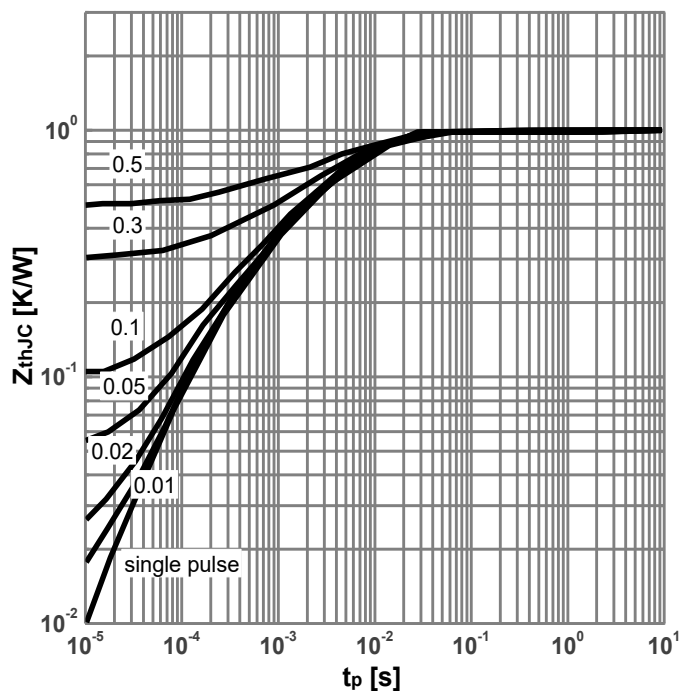
5. Electrical Characteristics Diagrams

Diagram 1: Power dissipation



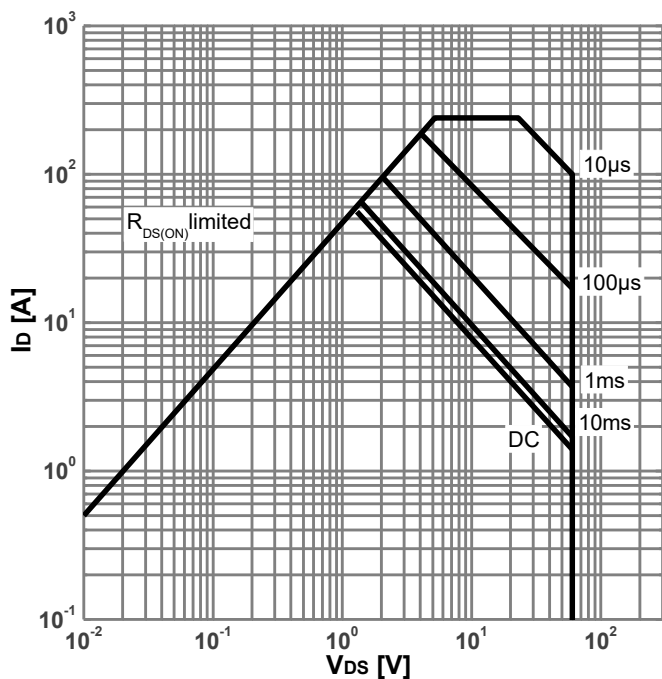
$$P_{tot}=f(T_c)$$

Diagram 2: Max. transient thermal impedance



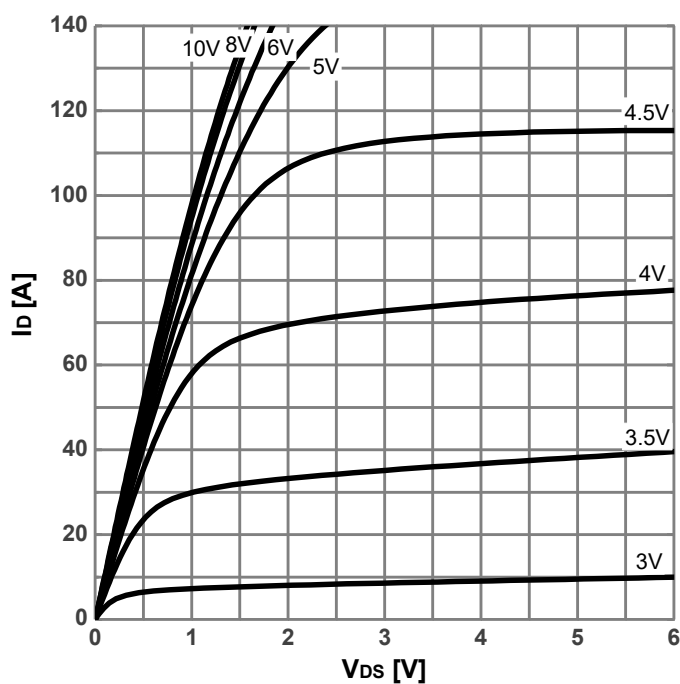
$$Z_{thJC}=f(t_p); \text{ parameter: } D= t_p/T$$

Diagram 3: Safe operating area



$$I_D=f(V_{DS}); T_J=25^{\circ}\text{C}; D=0; \text{ parameter: } t_p$$

Diagram 4: Typ. output characteristics



$$I_D=f(V_{DS}); T_J=25^{\circ}\text{C}; \text{ parameter: } V_{GS}$$

Diagram 5: Typ. output characteristics

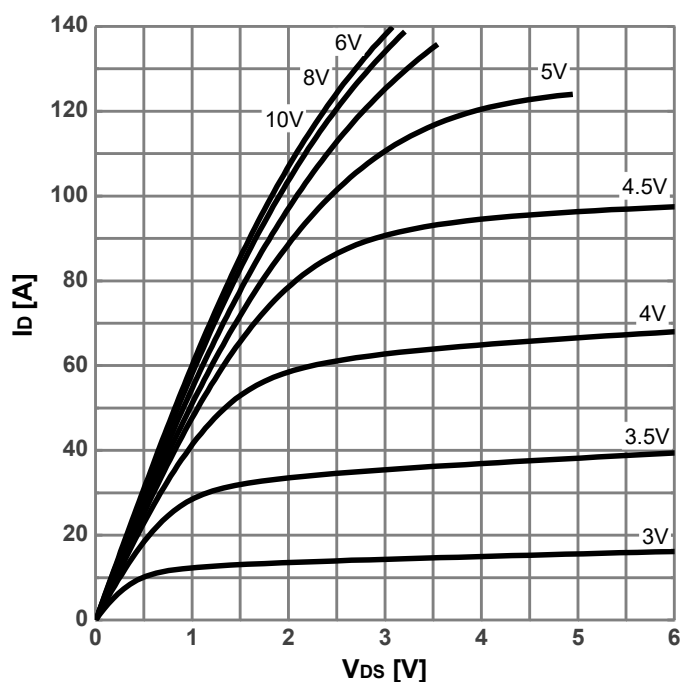

 $I_D = f(V_{DS}); T_j = 125^\circ\text{C}; \text{parameter: } V_{GS}$

Diagram 6: Typ. transfer characteristics

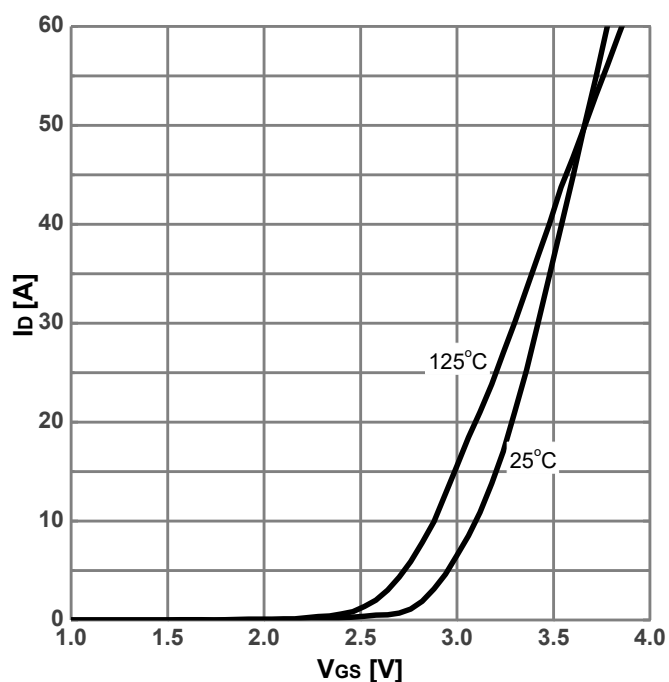

 $I_D = f(V_{GS}); V_{DS} = 15\text{V}; \text{parameter: } T_j$

Diagram 7: Gate threshold voltage vs. Junction temperature

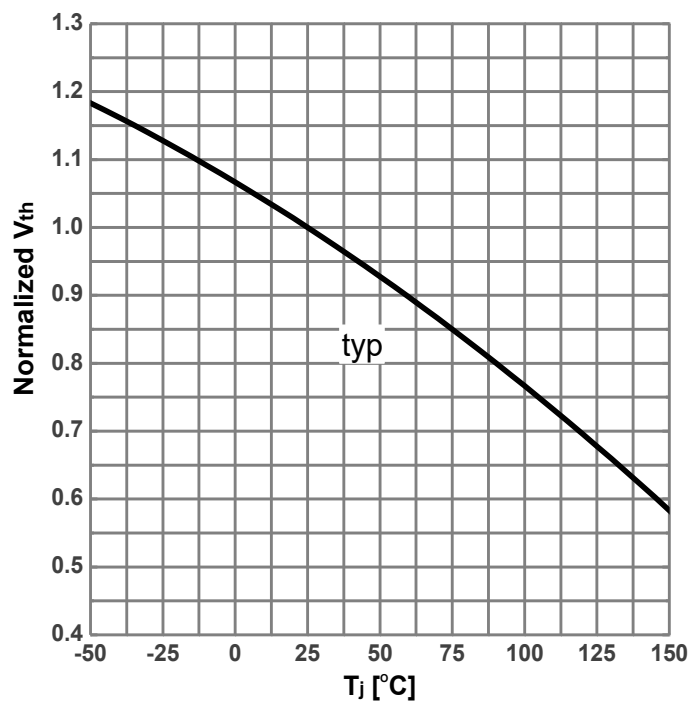

 $V_{th} = f(T_j); I_D = 250\mu\text{A}$

Diagram 8: On-state resistance vs. Drain current

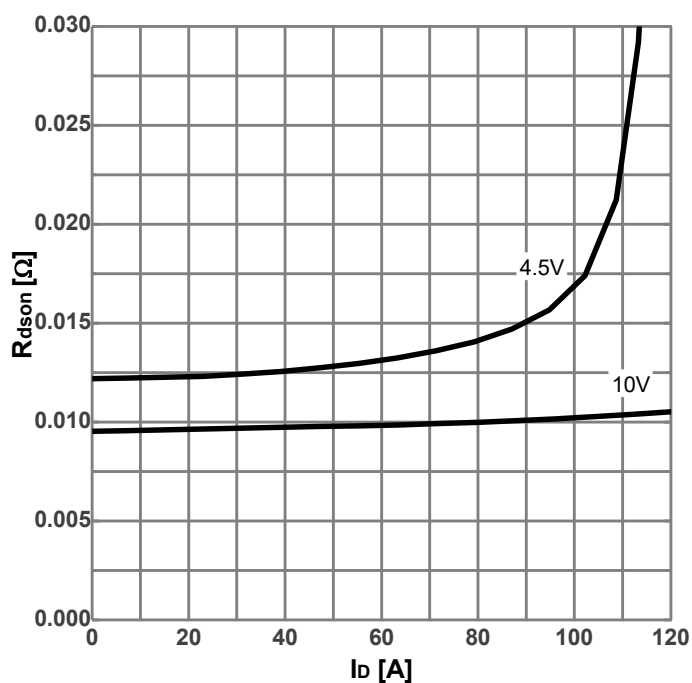
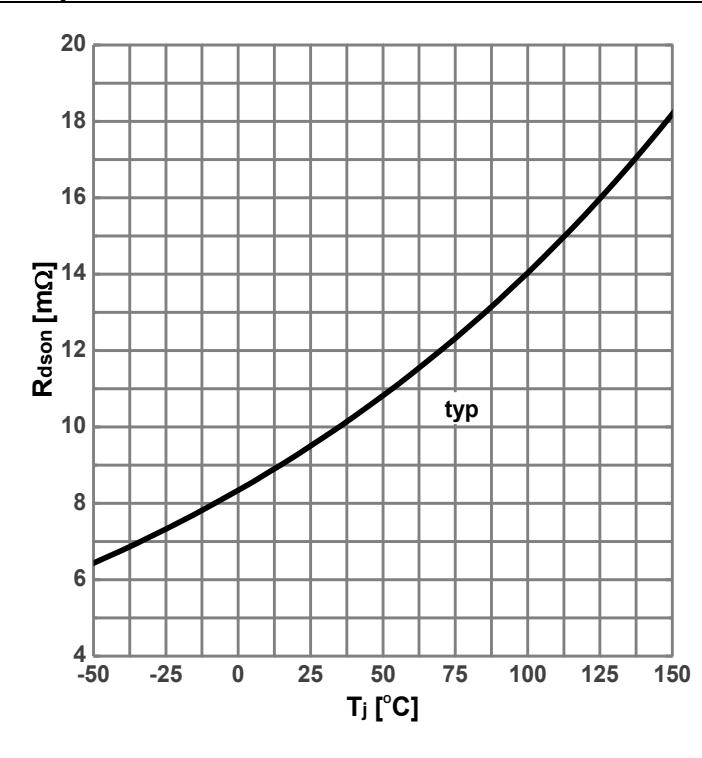
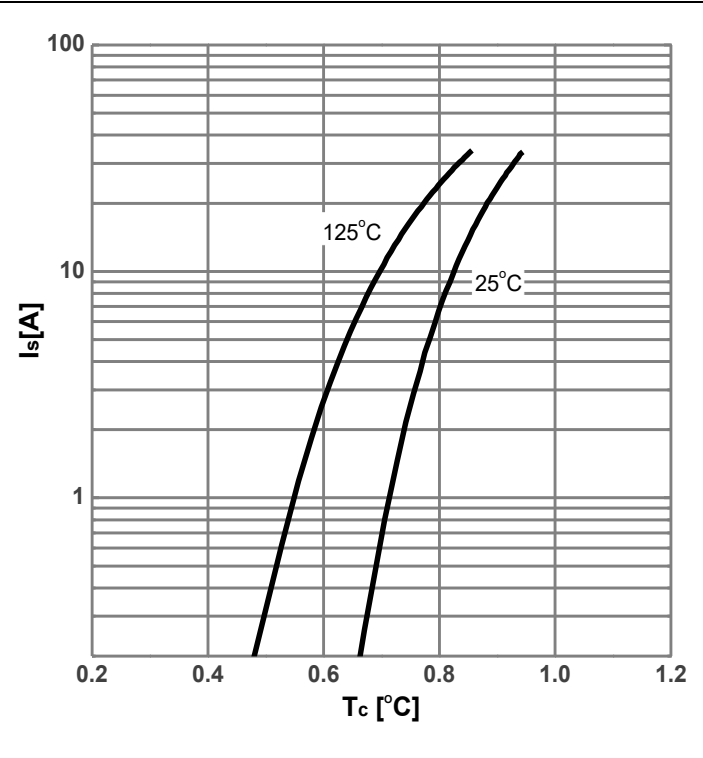

 $R_{DS(on)} = f(I_D); T_j = 25^\circ\text{C}; \text{parameter: } V_{GS}$

Diagram 9: On-state resistance vs. Junction temperature



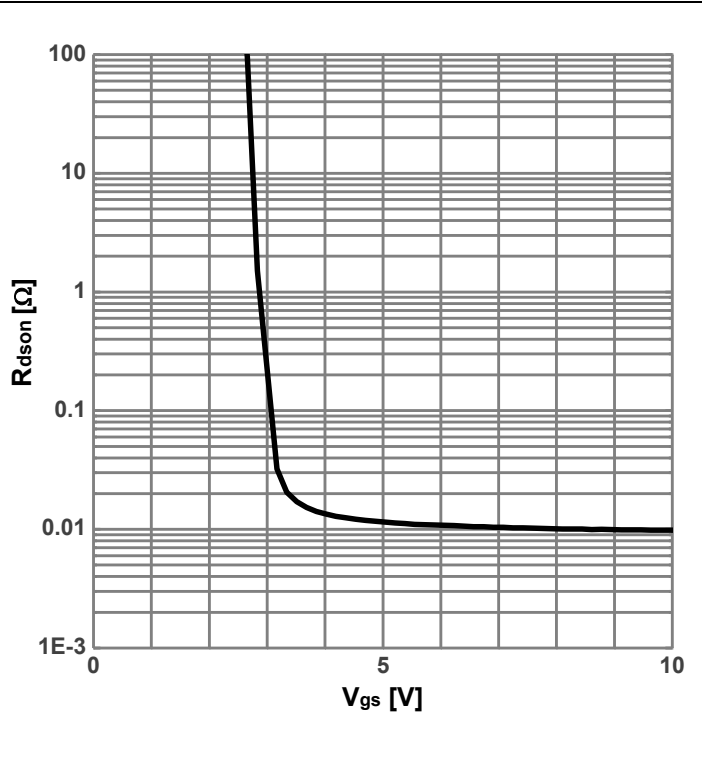
$R_{DS(on)}=f(T_j)$; $I_D=15A$; $V_{GS}=10V$

Diagram 10: Forward characteristics of reverse diode



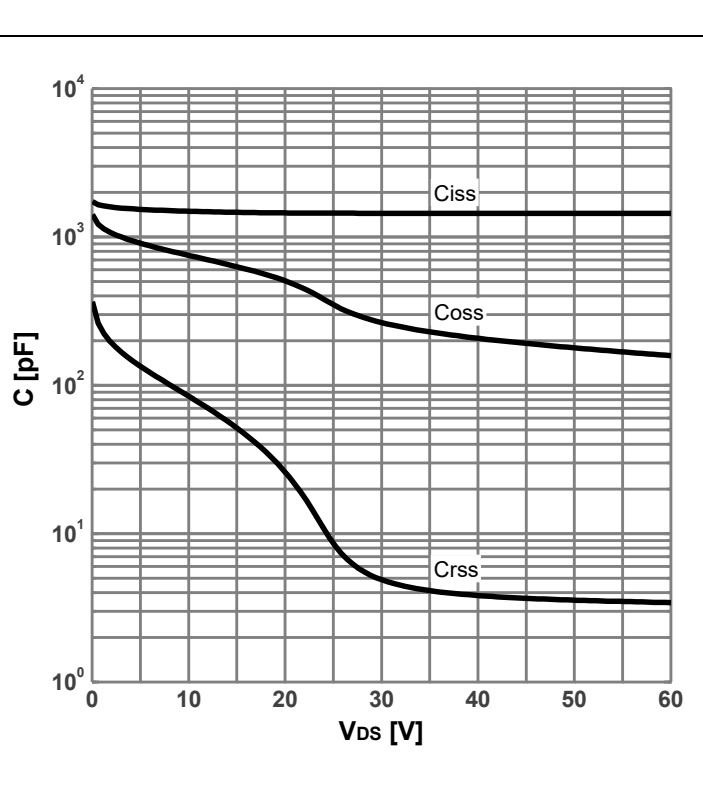
$I_F=f(V_{SD})$; parameter: T_j

Diagram 11: On-state resistance vs. Vgs characteristics

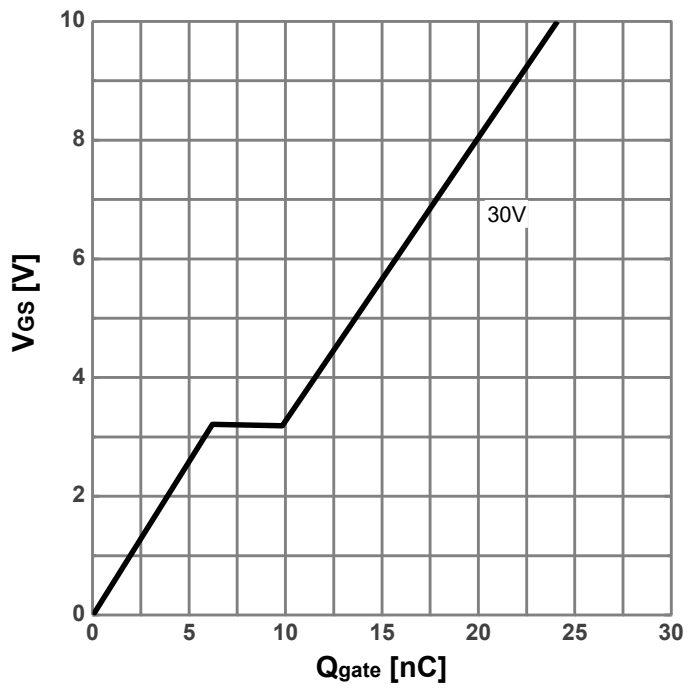


$R_{DS(on)}=f(V_{GS})$; $T_j=25^{\circ}C$; $I_D=15A$

Diagram 12: Typ. capacitances



$C=f(V_{DS})$; $V_{GS}=0V$; $f=1MHz$

Diagram 13: Typ. gate charge

$V_{GS}=f(Q_{gate})$; $I_D=14.5A$ pulsed; $V_{DS}=30V$

6. Test Circuits

Table 7. Diode Characteristics

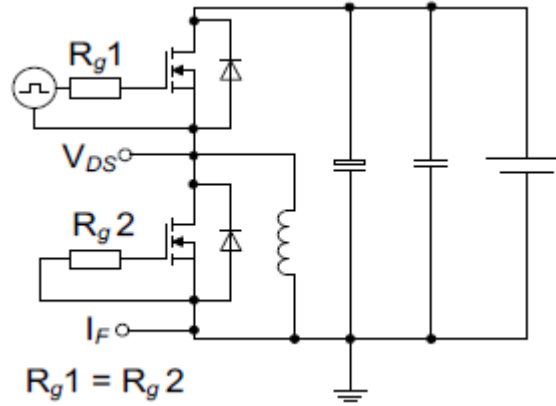
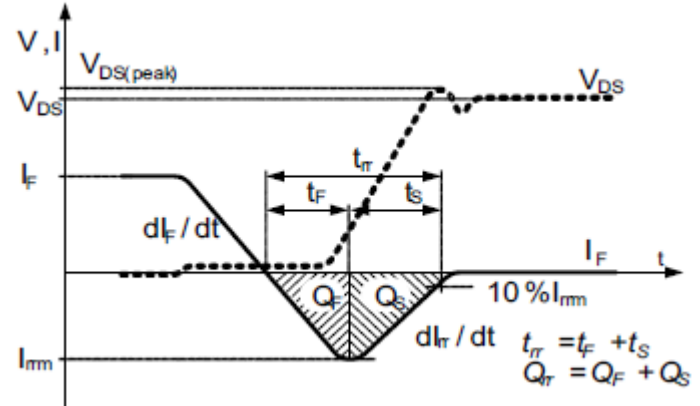
Test circuit for diode characteristics	Diode recovery waveform
	

Table 8. Switching Times

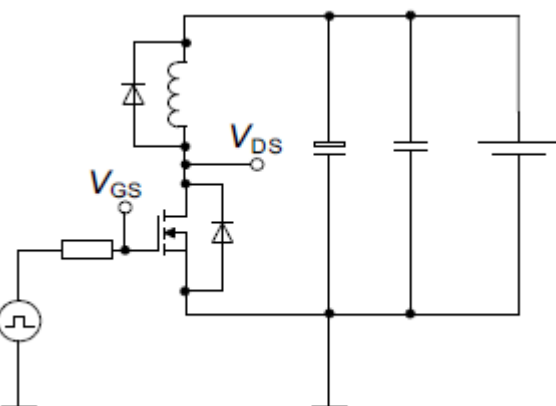
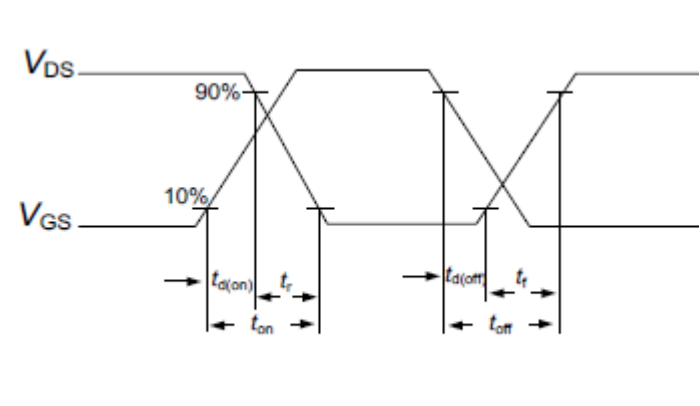
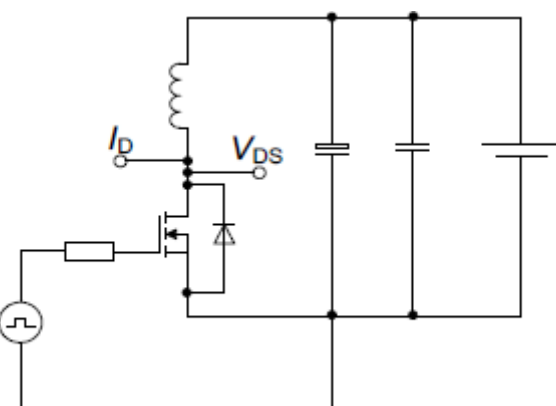
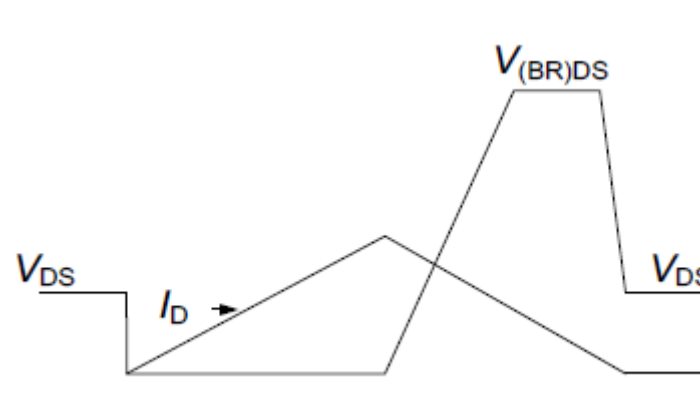
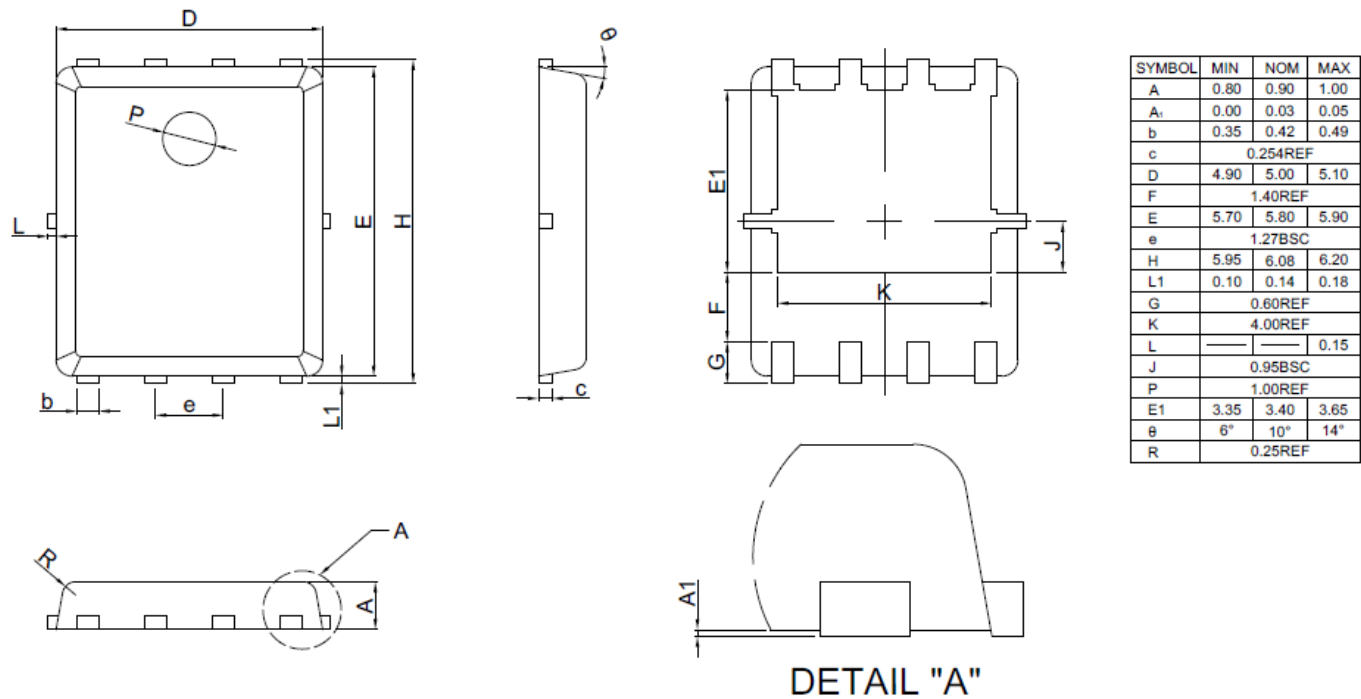
Switching times test circuit for inductive load	Switching times waveform
	

Table 9. Unclamped Inductive Load

Unclamped inductive load test circuit	Unclamped inductive waveform
	

7. Package Outlines

Figure 1 Outline DFN5*6 Dimensions in mm



8. Appendix

CoolSemi Webpage: www.coolsemi.com.