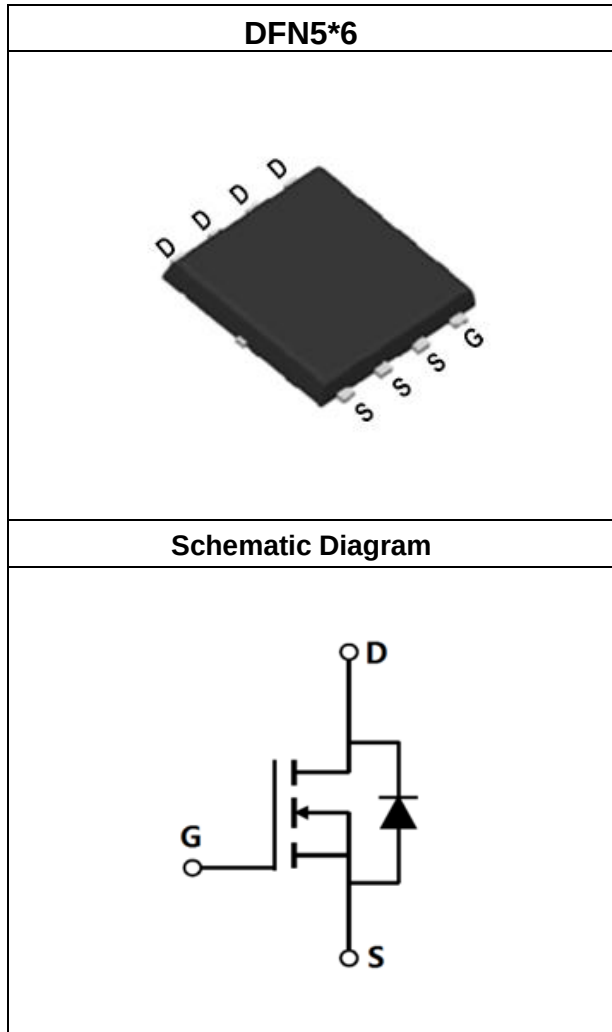


N-channel 60V, 7.5mΩ typ.,
SGT MOSFET S2 in DFN5*6

Datasheet - production data

1. Descriptions



Key Performance Parameters

Parameters	Value	Unit
BV_{DSS}	60	V
$R_{DS(on),max}$	9	mΩ
P_D	62.5	W
I_D	60	A

Features

- High Speed Power Switching, Logic level
- Enhanced Body diode dv/dt capability
- Enhanced Avalanche Ruggedness
- 100% UIS Tested, 100% Rg Tested
- Lead Free, Halogen Free

Applications

- DC/DC Converter
- Motor Drivers
- Ideal for high-frequency switching and synchronous rectification

Type/Ordering Code	Package	Marking	Related Links
CSLS090N06S2H	DFN5*6	090N06S2H	see Appendix A

Contents

1.	Descriptions	1
2.	Maximum Ratings	3
3.	Thermal Characteristics	3
4.	Electrical Characteristics	4
5.	Electrical Characteristics Diagrams	5
6.	Test Circuits	9
7.	Package Outlines	10
8.	Appendix	11

2. Maximum Ratings

at $T_j = 25^\circ\text{C}$, unless otherwise specified

Absolute Maximum Ratings

Symbol	Parameter	Values			Unit	Test Condition
		Min.	Typ.	Max.		
V_{DS}	Drain-source voltage	-	-	60	V	$V_{GS}=0V$, $I_D=250\mu A$
V_{GS}	Gate source voltage	-20	-	20	V	static; AC ($f>1\text{ Hz}$)
I_D	Continuous drain current	-	-	60 43	A	$T_C=25^\circ\text{C}$ $T_C=100^\circ\text{C}$
$I_{D,pulse}$	Pulsed drain current	-	-	240	A	$T_C=25^\circ\text{C}$
P_D	Power dissipation DFN5*6	-	-	62.5	W	$T_C=25^\circ\text{C}$
E_{AS}	Avalanche energy, single pulse ¹⁾	-	-	180	mJ	$I_D=6A$; $V_{DD}=50V$
T_j, T_{stg}	Operating and storage temperature	-55	-	150	$^\circ\text{C}$	-

3. Thermal Characteristics

Thermal Characteristics (DFN5*6)

Symbol	Parameter	Values			Unit	Test Condition
		Min.	Typ.	Max.		
R_{thJC}	Thermal resistance, junction - case	-	-	2	$^\circ\text{C/W}$	$T_C = 25^\circ\text{C}$
R_{thJA}	Thermal resistance, junction - ambient	-	-	75	$^\circ\text{C/W}$	$T_C = 25^\circ\text{C}$

4. Electrical Characteristics

at $T_j = 25^\circ\text{C}$, unless otherwise specified

Symbol	Parameter	Values			Unit	Test Condition
		Min.	Typ.	Max.		

Off Characteristics

$V_{(BR)DSS}$	Drain-source breakdown voltage	60	-	-	V	$V_{GS}=0V, I_D=250\mu A$
I_{DSS}	Zero gate voltage drain current	-	-	1	μA	$V_{DS}=60V, V_{GS}=0V$
I_{GSS}	Gate-source leakage current	-	-	± 100	nA	$V_{GS}=\pm 20V, V_{DS}=0V$

On Characteristics³⁾

$V_{(GS)th}$	Gate threshold voltage	2.0	2.6	4.0	V	$V_{DS}=V_{GS}, I_D=250\mu A$
$R_{DS(on)}$	Drain-source on-state resistance	-	7.5 10	9 14	m Ω	$V_{GS}=10V, I_D=20A$ $V_{GS}=4.5V, I_D=10A$
R_G	Gate resistance	-	2.6	-	Ω	$V_{DD}=0V, V_{GS}=0V, F=1MHz$
g_{fs}	Transconductance	-	80	-	S	$V_{DS}=5V, I_D=20A$

Dynamic Characteristics

C_{iss}	Input capacitance	-	1480	-	pF	$V_{GS}=0V, V_{DS}=30V,$ $F=1MHz$
C_{oss}	Output capacitance	-	290	-	pF	
C_{rss}	Reverse transfer capacitance	-	4.1	-	pF	

Switching Characteristics⁴⁾

$t_{d(on)}$	Turn-on delay time	-	11	-	ns	$V_{DD}=30V, V_{GS}=10V,$ $I_D=14.5A, R_G=3\Omega$
t_r	Turn-on rise time	-	5	-	ns	
$t_{d(off)}$	Turn-off delay time	-	56	-	ns	
t_f	Turn-off fall time	-	12	-	ns	
Q_g	Gate charge total	-	23	-	nC	$V_{DD}=30V, I_D=14.5A, V_{GS}=10V$
Q_{gs}	Gate to source charge	-	4.8	-	nC	
Q_{gd}	Gate to drain charge	-	2.4	-	nC	

Reverse Diode Characteristics

V_{SD}	Diode forward voltage ³⁾	-	0.9	1.2	V	$V_{GS}=0V, I_F=20A$
I_S	Diode forward current ²⁾	-	-	60	A	
t_{rr}	Reverse recovery time	-	32	-	ns	$V_{GS}=0V, I_F=14.5A,$ $di/dt=100A/\mu s^3)$
Q_{rr}	Reverse recovery charge	-	46	-	μC	

1) $V_{DD}=50V, L=10mH, R_G=25\Omega$, Starting $T_j=25^\circ\text{C}$.

2) Surface Mounted on FR4 Board, $t \leq 10$ sec.

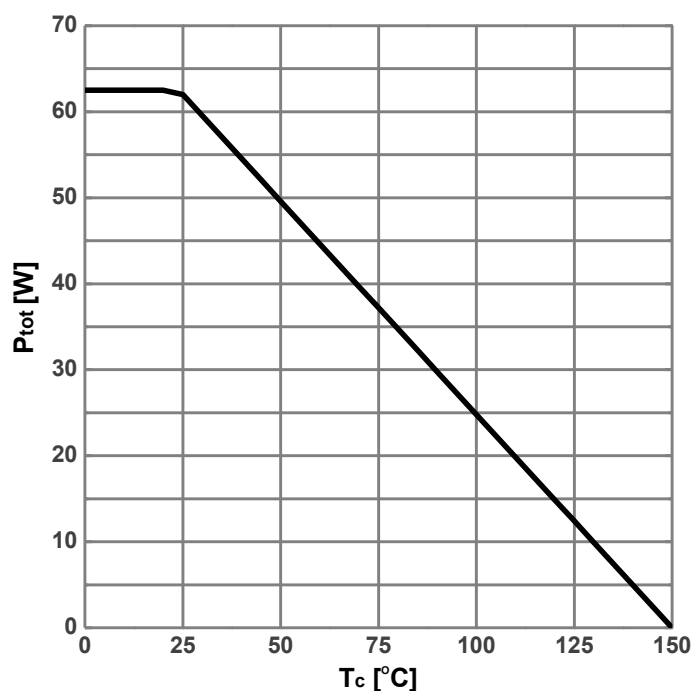
3) Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.

4) Guaranteed by design, not subject to production

5) Repetitive Rating: Pulse width limited by maximum junction temperature.

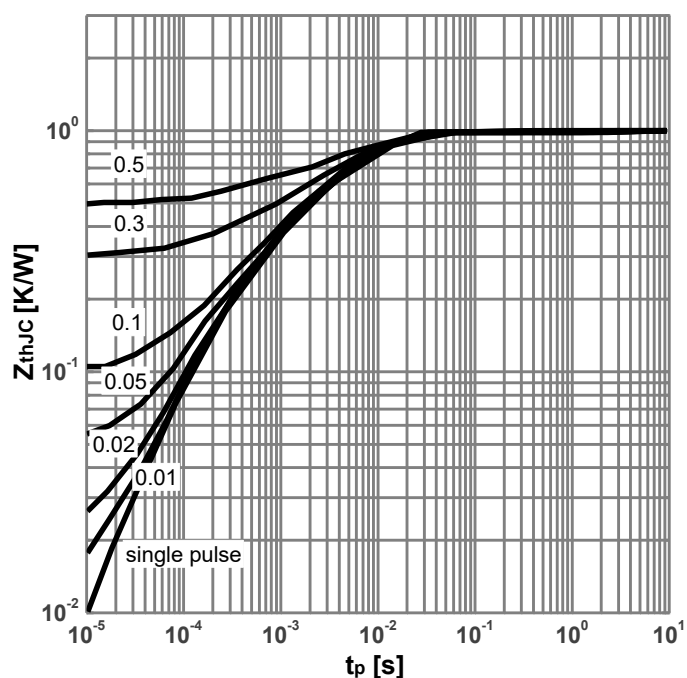
5. Electrical Characteristics Diagrams

Diagram 1: Power dissipation (DFN5*6)



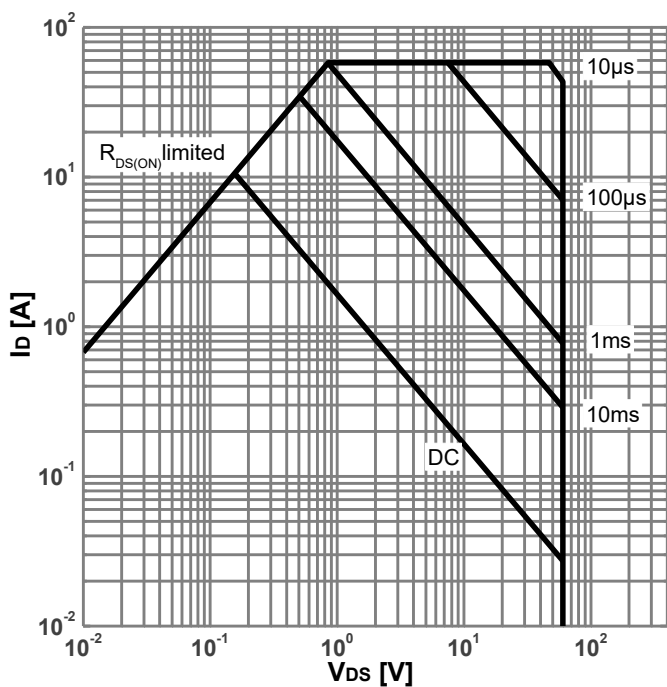
$$P_{\text{tot}} = f(T_c)$$

Diagram 2: Max. transient thermal impedance (DFN5*6)



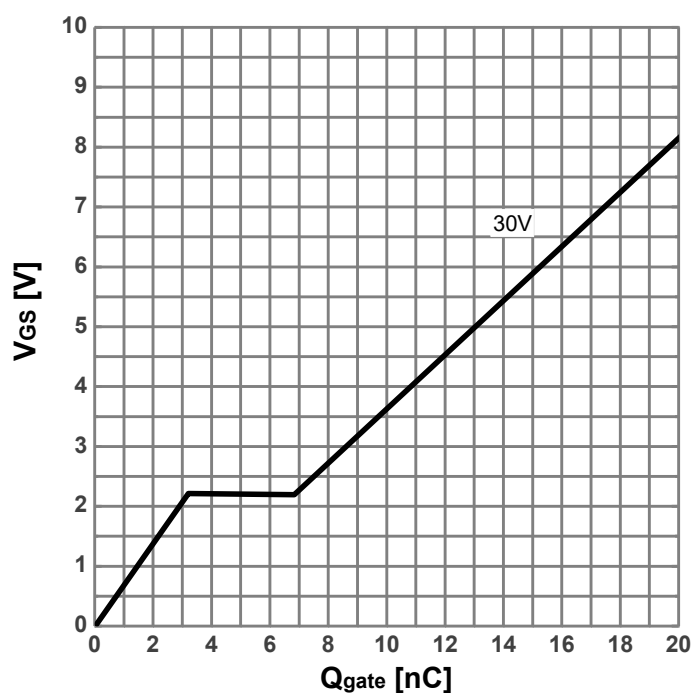
$$Z_{\text{thJC}} = f(t_p); \text{ parameter: } D = t_p/T$$

Diagram 3: Safe operating area (DFN5*6)



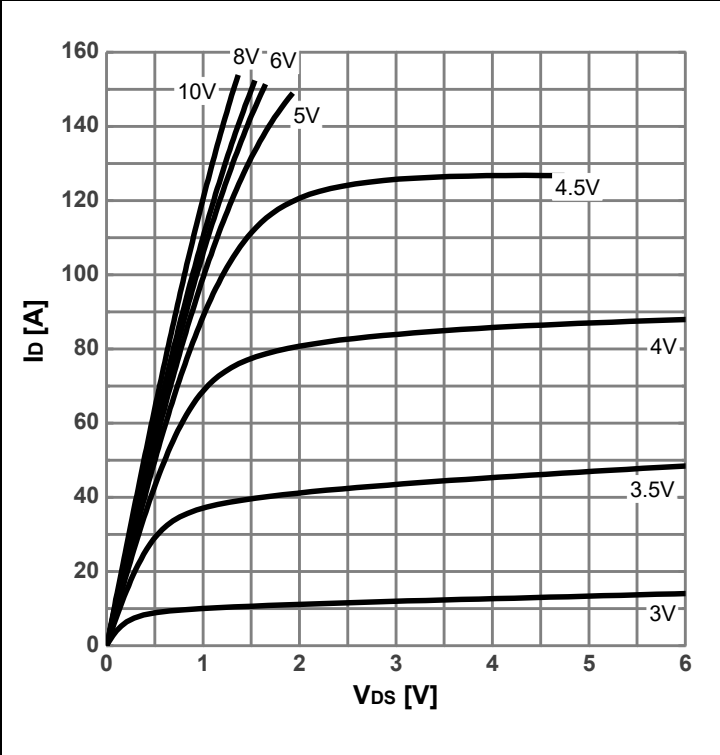
$$I_D = f(V_{DS}); T_J = 25^\circ\text{C}; D = 0; \text{ parameter: } t_p$$

Diagram 4: Typ. gate charge



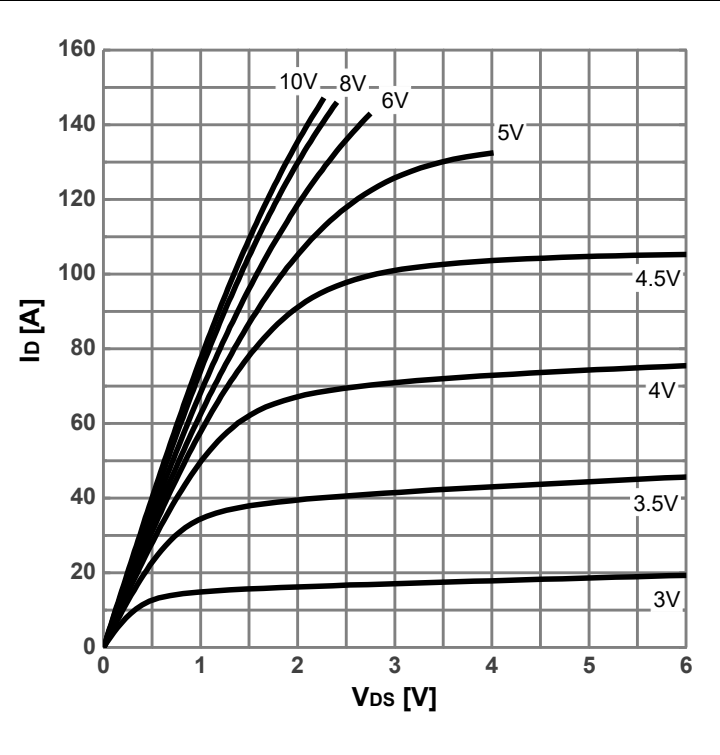
$$V_{GS} = f(Q_{\text{gate}}); I_D = 14.5\text{A pulsed}; V_{DS} = 30\text{V}$$

Diagram 5: Typ. output characteristics



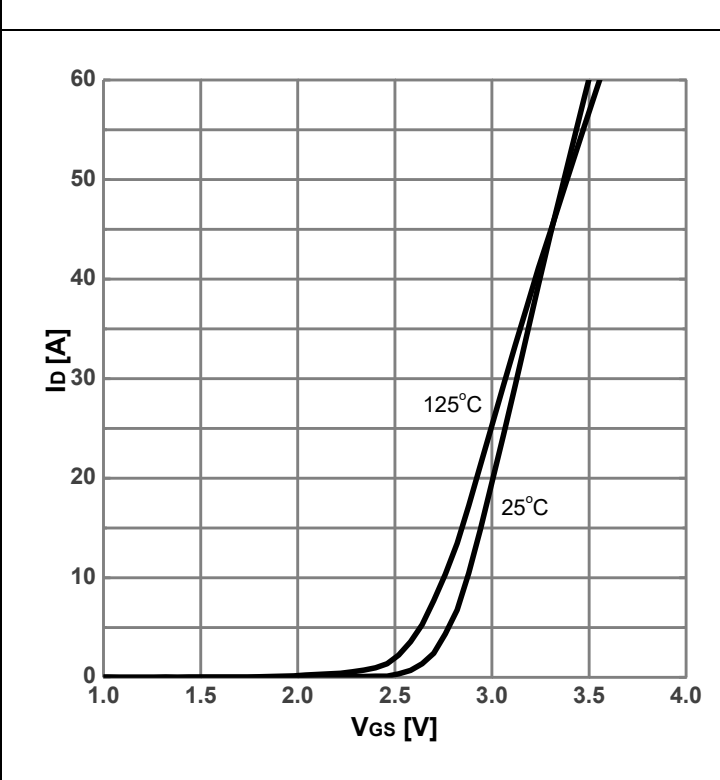
$I_D=f(V_{DS})$; $T_J=25^\circ\text{C}$; parameter: V_{GS}

Diagram 6: Typ. output characteristics



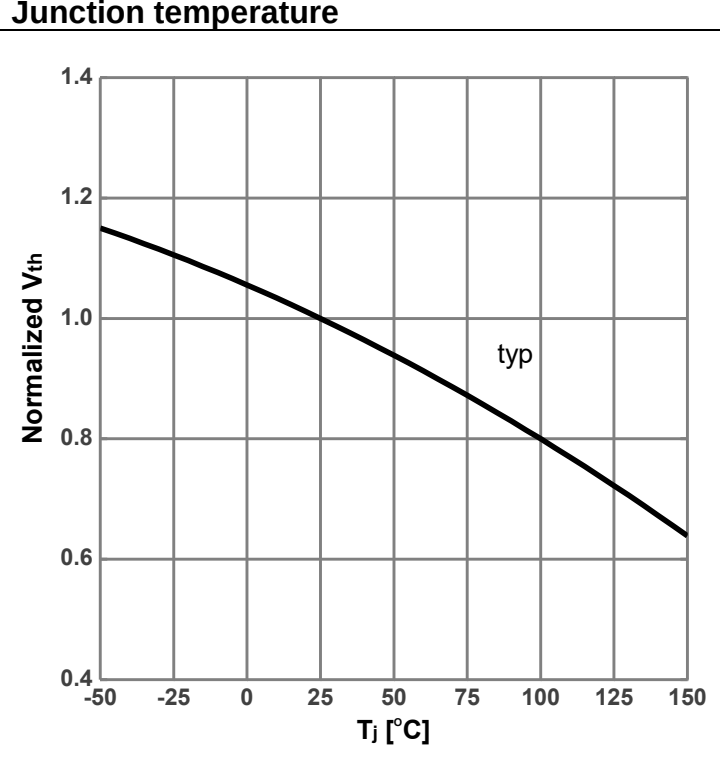
$I_D=f(V_{DS})$; $T_J=125^\circ\text{C}$; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



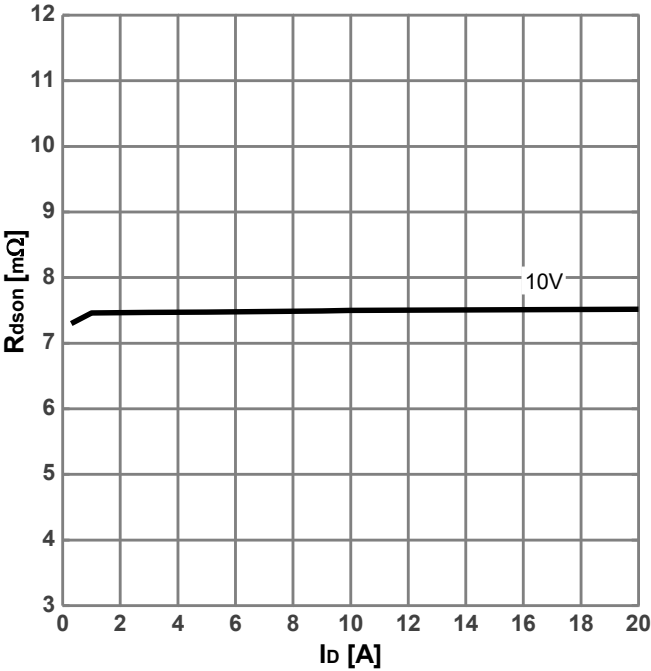
$I_D=f(V_{GS})$; $V_{DS}=15\text{V}$; parameter: T_J

Diagram 8: Gate threshold voltage vs. Junction temperature



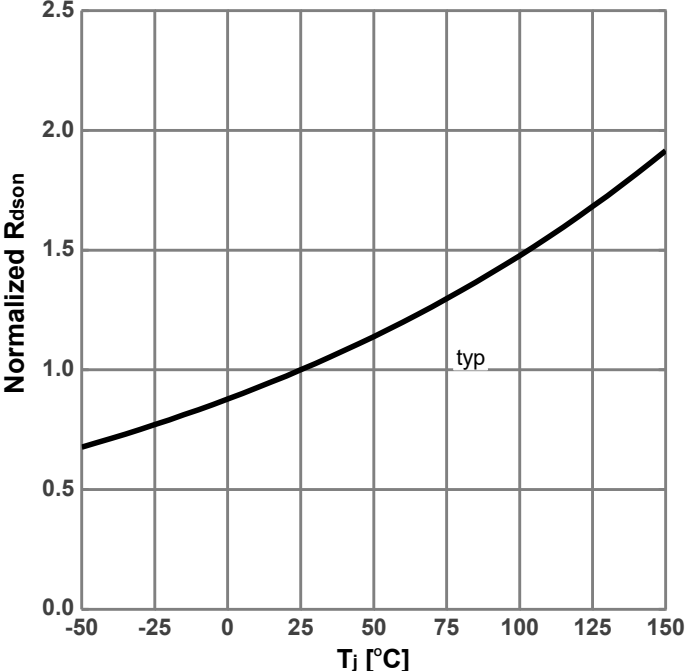
$V_{th}=f(T_J)$; $I_D=250\mu\text{A}$

Diagram 9: On-state resistance vs. Drain current



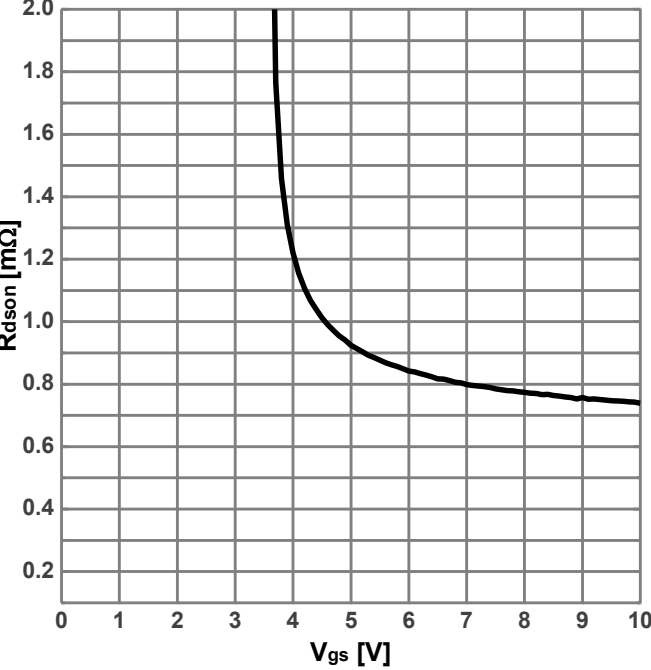
$R_{DS(on)}=f(I_D)$; $T_J=25^\circ C$; parameter: V_{GS}

Diagram 10: On-state resistance vs. Junction temperature



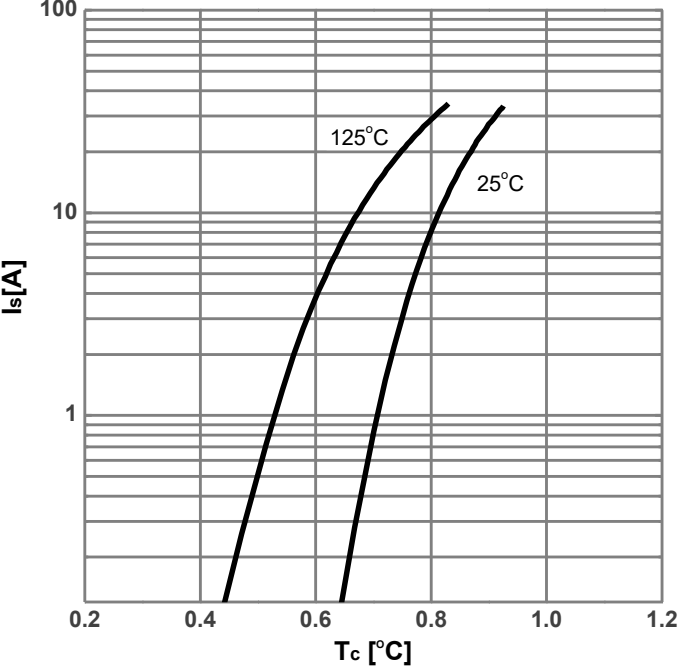
$R_{DS(on)}=f(T_J)$; $I_D=20A$; $V_{GS}=10V$

Diagram 11: On-state resistance vs. Vgs characteristics

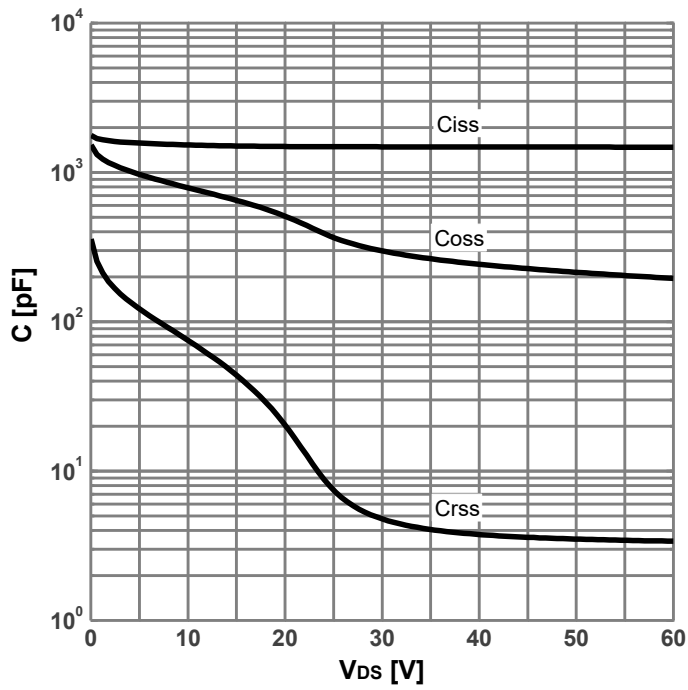


$R_{DS(on)}=f(V_{GS})$; $T_J=25^\circ C$; $I_D=20A$

Diagram 12: Forward characteristics of reverse diode



$I_F=f(V_{SD})$; parameter: T_J

Diagram 13: Typ. capacitances $C=f(V_{DS}); V_{GS}=0V; f=1MHz$

6. Test Circuits

Table 7. Diode Characteristics

Test circuit for diode characteristics $R_{g1} = R_{g2}$	Diode recovery waveform $t_{rr} = t_f + t_s$ $Q_{tr} = Q_F + Q_S$
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Table 8. Switching Times

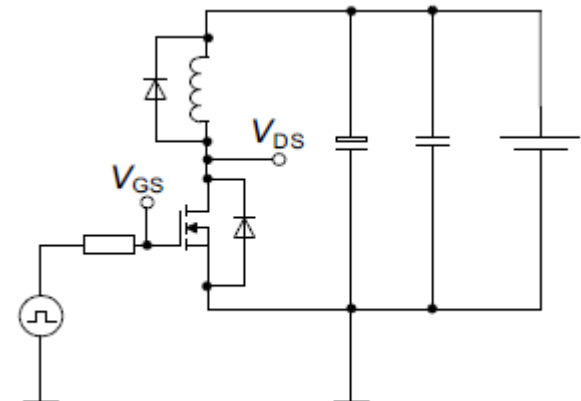
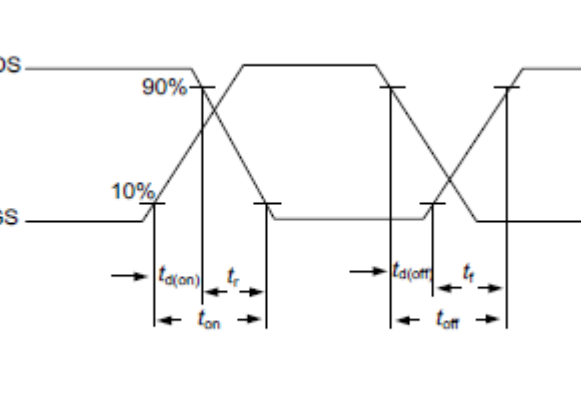
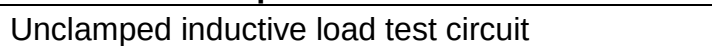
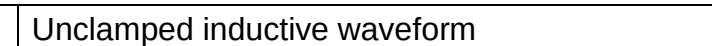
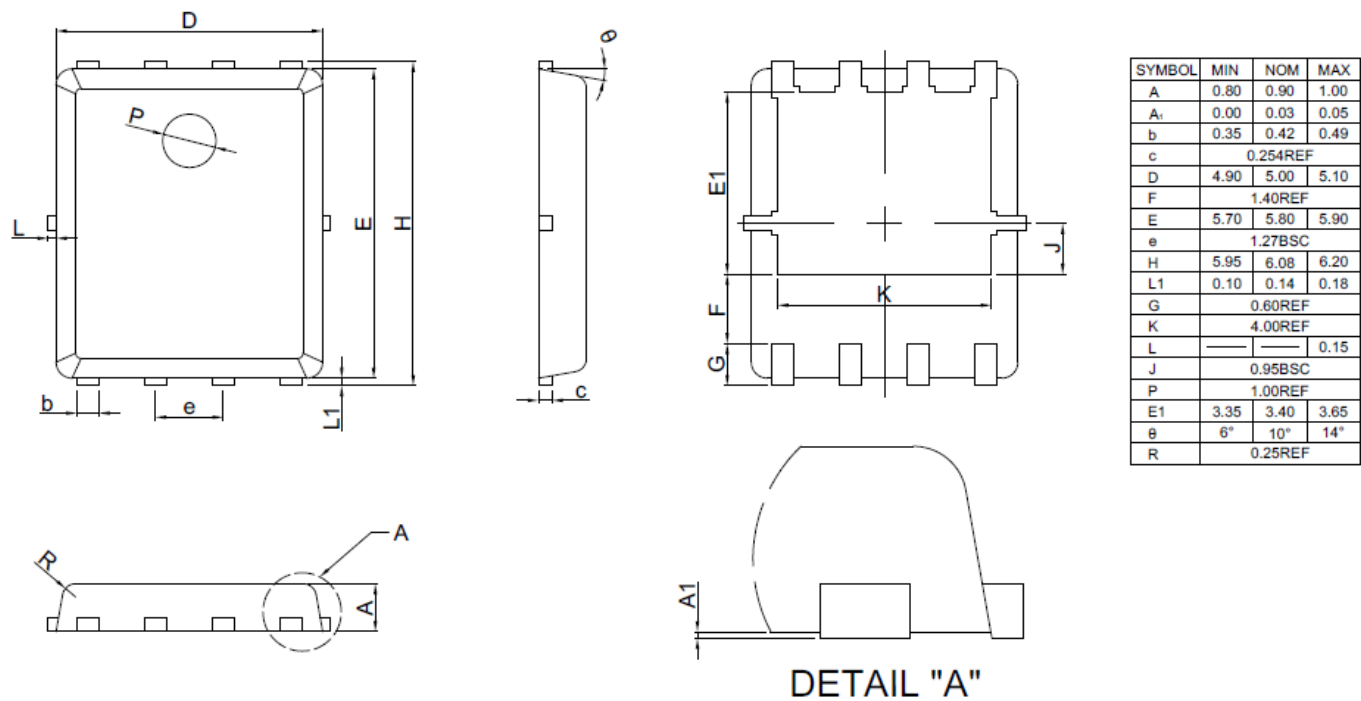
Switching times test circuit for inductive load	Switching times waveform
	

Table 9. Unclamped Inductive Load

Unclamped inductive load test circuit 	Unclamped inductive waveform 
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7. Package Outlines

Figure 1 Outline DFN5*6 Dimensions in mm



8. Appendix

CoolSemi Webpage: www.coolsemi.com.