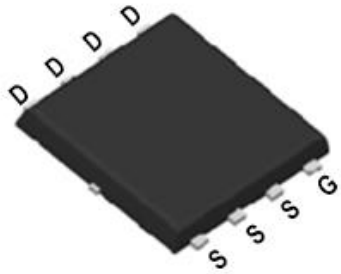
N-channel 80V, 3.8mΩ max.,
SGT MOSFET S2 in DFN5*6

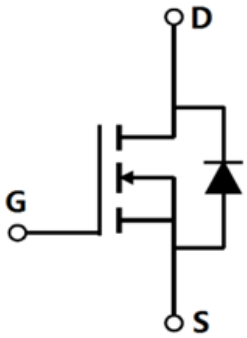
Datasheet - production data

1. Descriptions

DFN5*6



Schematic Diagram



Key Performance Parameters

Parameters	Value	Unit
BV_{DSS}	80	V
$R_{DS(on),max}$	3.8	mΩ
P_D	114	W
$I_{D(Package\ Limited)}$	60	A

Features

- High Speed Power Switching,Logic level
- Enhanced Body diode dv/dt capability
- Ehanced Avalanche Ruggedness
- 100% UIS Tested, 100% Rg Tested
- Lead Free, Halogen Free

Applications

- DC/DC Converter
- Motor Drivers
- Ideal for high-frequency switching and synchronous rectification

Type/Ordering Code	Package	Marking	Related Links
CSLS038N08S2	DFN5*6	038N08S2	see Appendix A

Contents

2. Maximum Ratings

at T_j = 25°C, unless otherwise specified

Absolute Maximum Ratings

Symbol	Parameter	Values			Unit	Test Condition
		Min.	Typ.	Max.		
V_{DS}	Drain-source voltage	-	-	80	V	V_{GS}=0V, I_D=250μA
V_{GS}	Gate source voltage	-20	-	20	V	static; AC (f>1 Hz)
I_D	Continuous drain current(Sillicon Limited)	-	-	187	A	T_C=25°C
	Continuous drain current (Package Limited)	-	-	60	A	T_C=25°C
$I_{D,pulse}$	Pulsed drain current	-	-	400	A	T_C=25°C
P_D	Power dissipation DFN5*6	-	-	114	W	T_C=25°C
E_{AS}	Avalanche energy, single pulse[1)]	-	-	600	mJ	I_D=49A; V_{DD} =50V
T_j, T_{stg}	Operating and storage temperature	-55	-	150	°C	-

3. Thermal Characteristics

Thermal Characteristics (DFN5*6)

Symbol	Parameter	Values			Unit	Test Condition
		Min.	Typ.	Max.		
R_{thJC}	Thermal resistance, junction - case	-	-	1.1	°C/W	T_C = 25°C
R_{thJA}	Thermal resistance, junction - ambient	-	-	55	°C/W	T_C = 25°C

4. Electrical Characteristics

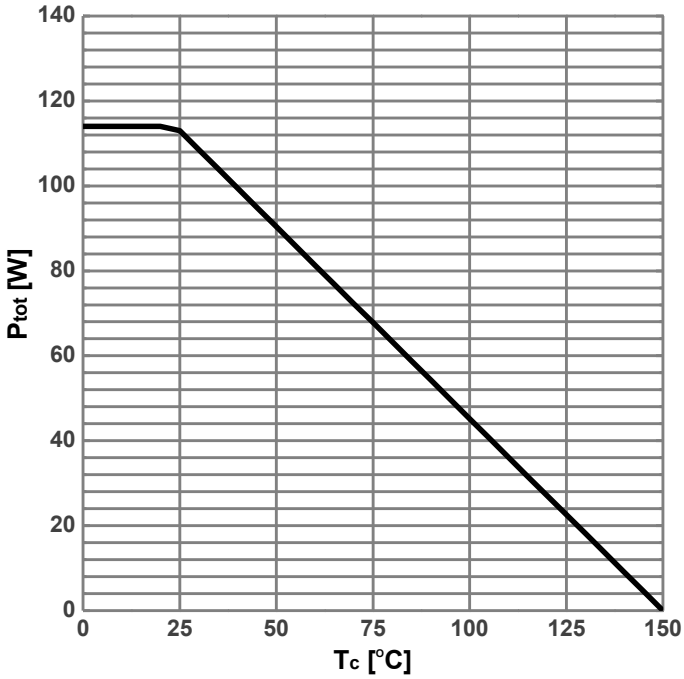
at T_j = 25°C, unless otherwise specified

Symbol	Parameter	Values			Unit	Test Condition
		Min.	Typ.	Max.		
Off Characteristics						
$V_{(BR)DSS}$	Drain-source breakdown voltage	80	-	-	V	V_{GS}=0V, I_D=250μA
I_{DSS}	Zero gate voltage drain current	-	-	1	μA	V_{DS}=80V, V_{GS}=0V, T_j=25°C
I_{GSS}	Gate-source leakage current	-	-	±100	nA	V_{GS}=±20V, V_{DS}=0V
On Characteristics[3)]						
$V_{(GS)th}$	Gate threshold voltage	2	3	4	V	V_{DS}=V_{GS}, I_D=250μA
$R_{DS(on)}$	Drain-source on-state resistance	-	3.3	3.8	mΩ	V_{GS}=10V, I_D=20A, T_j=25°C
R_G	Gate resistance	-	2	-	Ω	V_{DD}=0V,V_{GS}=0V,F=1MHz
g_{fs}	Transconductance		90		S	V_{DS}=5V, I_D=20A
Dynamic Characteristics						
C_{iss}	Input capacitance	-	4000	-	pF	V_{GS}=0V, V_{DS}=40V, F=1MHz
C_{oss}	Output capacitance	-	499	-	pF	
C_{rss}	Reverse transfer capacitance	-	26	-	pF	
Switching Characteristics[4)]						
$t_{d(on)}$	Turn-on delay time	-	25	-	ns	V_{DD}=40V, V_{GS}=10V, I_D=20A, R_G=10Ω
t_r	Turn-on rise time	-	55	-	ns	
$t_{d(off)}$	Turn-off delay time	-	75	-	ns	
t_f	Turn-off fall time	-	52	-	ns	
Q_g	Gate charge total	-	61	-	nC	V_{DD}=40V, I_D=25A, V_{GS}=0 to 10V
Q_{gs}	Gate to source charge	-	12.5	-	nC	
Q_{gd}	Gate to drain charge	-	12	-	nC	
Reverse Diode Characteristics						
V_{SD}	Diode forward voltage[3)]	-	0.82	-	V	V_{GS}=0V, I_F=20A
t_{rr}	Reverse recovery time	-	45	-	ns	V_R=40V, I_F=20A, di_F/dt=400A/μs
Q_{rr}	Reverse recovery charge	-	155	-	μC	

1) V_{DD}=50V, L=0.5mH, R_G=25Ω, Starting T_j=25°C.
2) Surface Mounted on FR4 Board, t ≤ 10 sec.
3) Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4) Guaranteed by design, not subject to production
5) Repetitive Rating: Pulse width limited by maximum junction temperature.

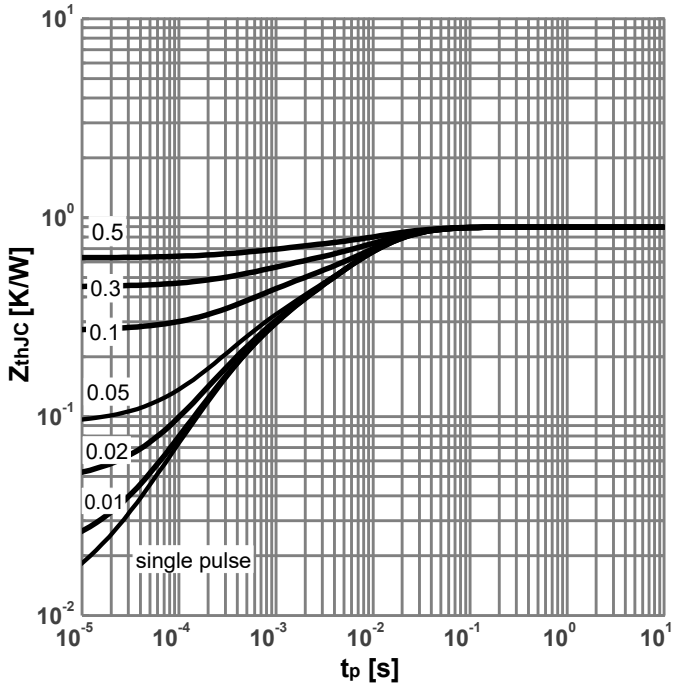
5. Electrical Characteristics Diagrams

Diagram 1: Power dissipation (DFN5*6)



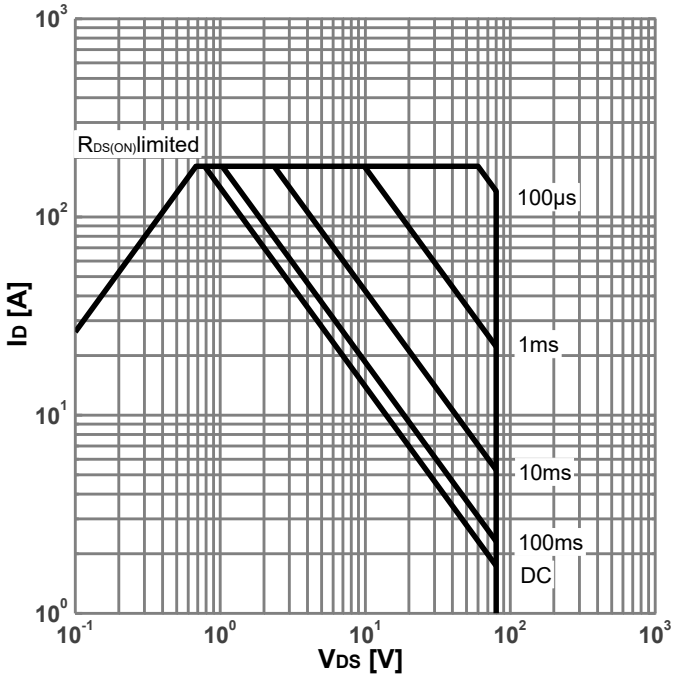
P_{tot}=f(T_C)

Diagram 2: Max. transient thermal impedance (DFN5*6)



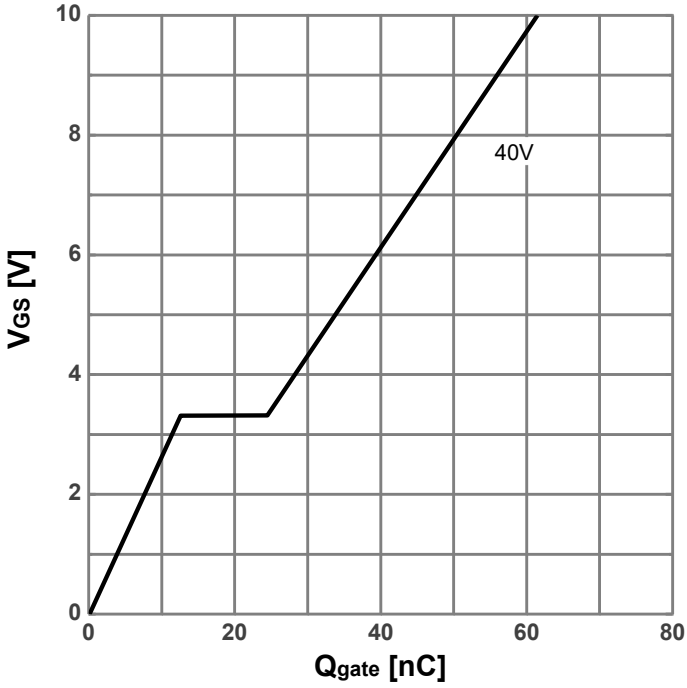
Z_{thJC}=f(t_p); parameter: D= t_p/T

Diagram 3: Safe operating area (DFN5*6)



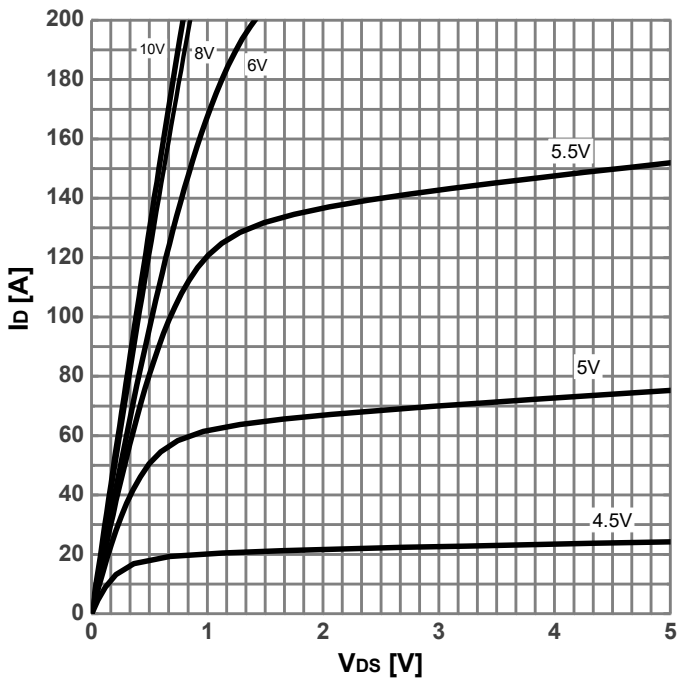
I_D=f(V_{DS}); Tj=25°C; D=0; parameter: t_p

Diagram 4: Typ. gate charge



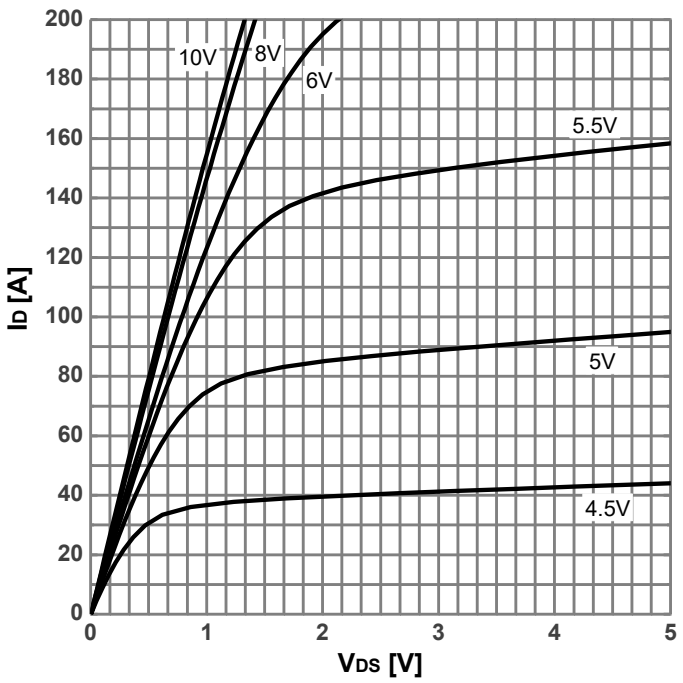
V_{GS}=f(Q_{gate}); I_D=25A pulsed; V_{DS}=40V

Diagram 5: Typ. output characteristics



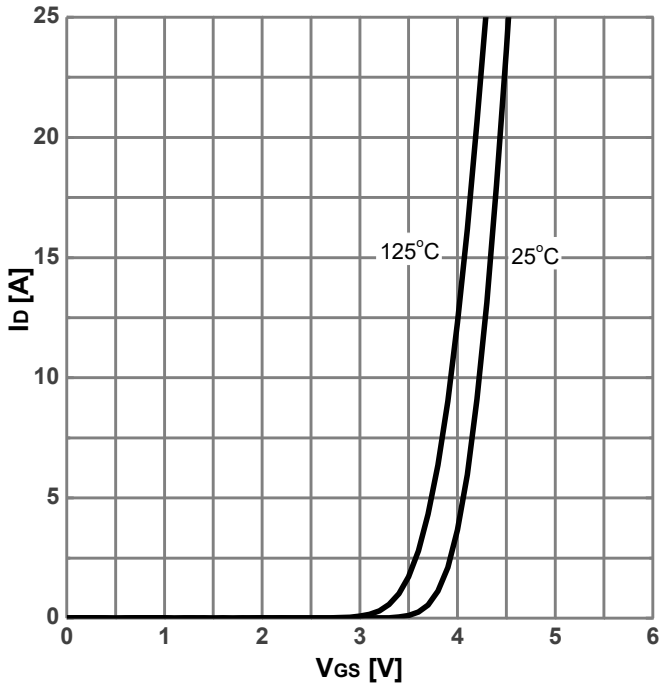
I_D=f(V_{DS}); Tj=25°C; parameter: V_{GS}

Diagram 6: Typ. output characteristics



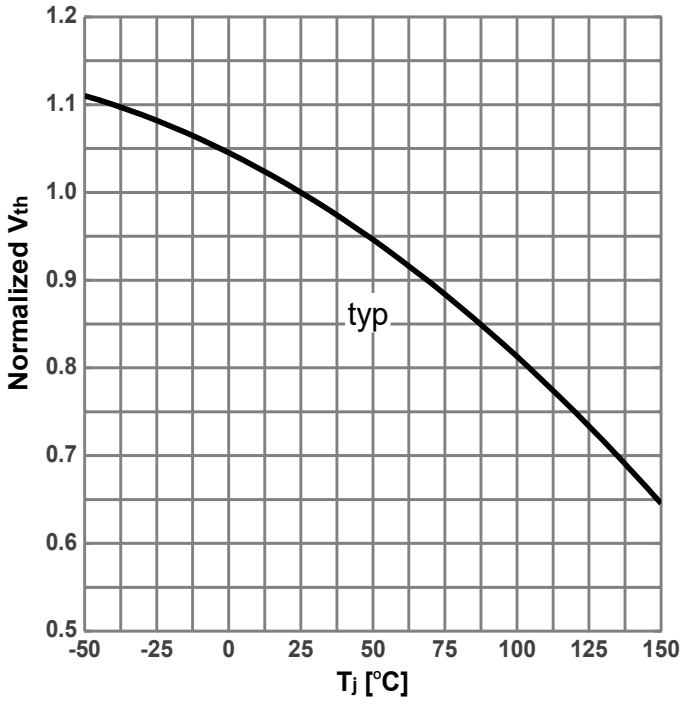
I_D=f(V_{DS}); Tj=125°C; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



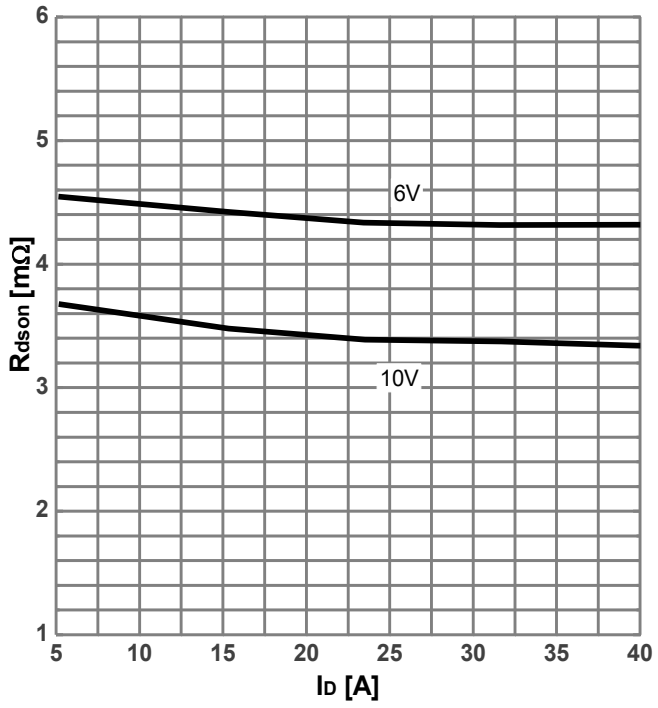
I_D=f(V_{GS}); V_{DS}=5V; parameter: T_j

Diagram 8: Gate threshold voltage vs. Junction temperature



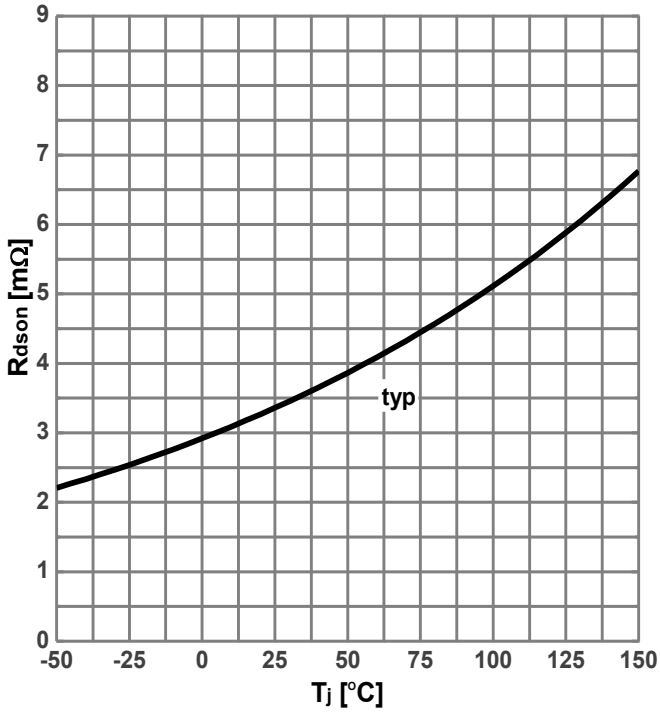
V_{th}=f(T_j); I_D=250µA

Diagram 9: On-state resistance vs. Drain current



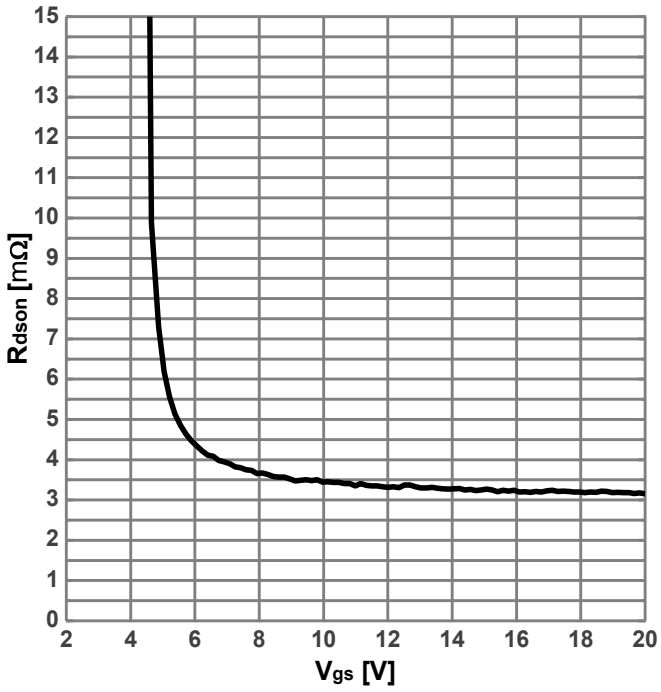
$R_{DS}(on)=f(I_D)$; $Tj=25°C$; parameter: V_{GS}

Diagram 10: On-state resistance vs. Junction temperature



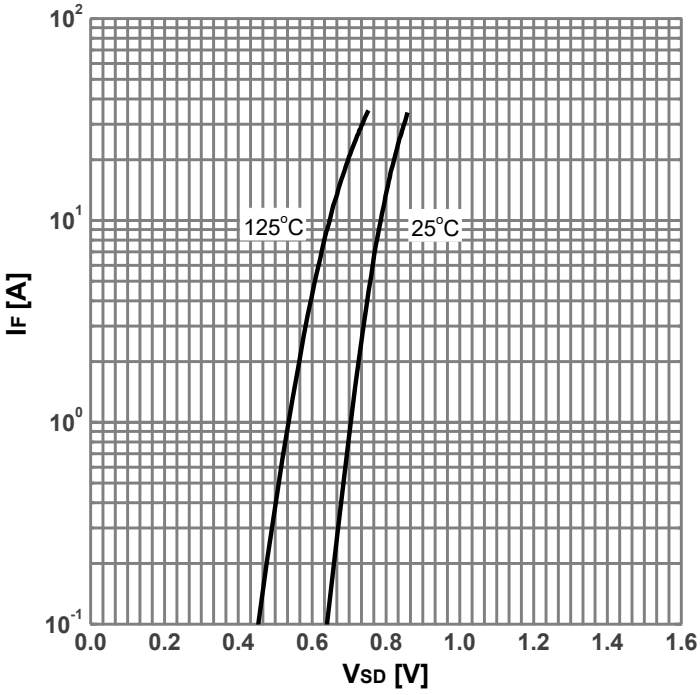
$R_{DS}(on)=f(T_j)$; $I_D=20A$; $V_{GS}=10V$

Diagram 11: On-state resistance vs. Vgs characteristics



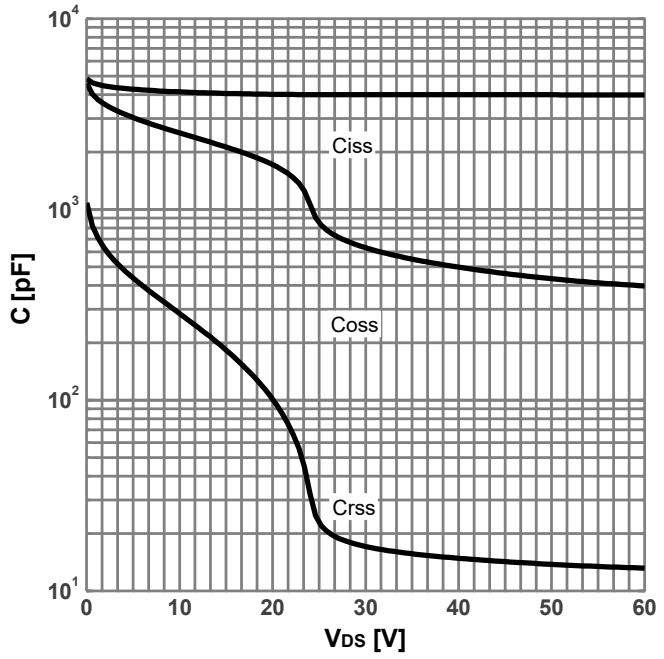
$R_{DS}(on)=f(V_{gs})$; $Tj=25°C$; $I_D=20A$

Diagram 12: Forward characteristics of reverse diode



$I_F=f(V_{SD})$; parameter: T_j

Diagram 13: Typ. capacitances



C=f(*V*DS); *V*GS=0V; f=1MHz

6. Test Circuits

Table 7. Diode Characteristics

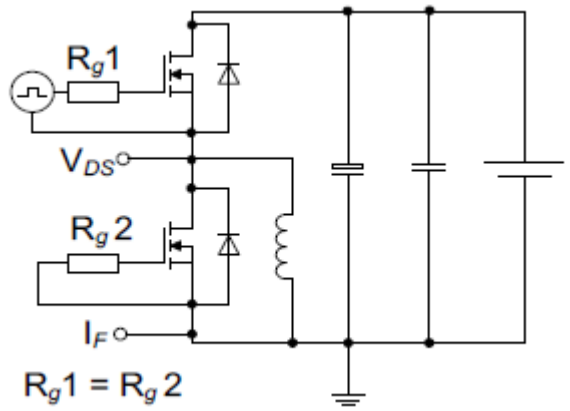
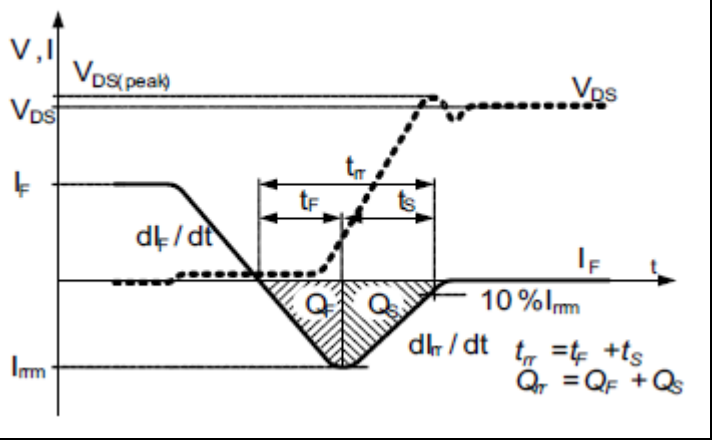
Test circuit for diode characteristics	Diode recovery waveform
	

Table 8. Switching Times

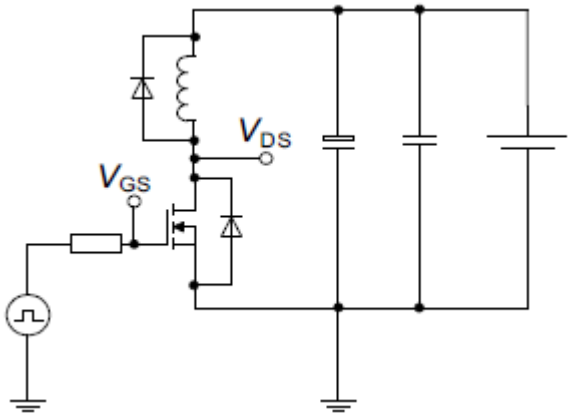
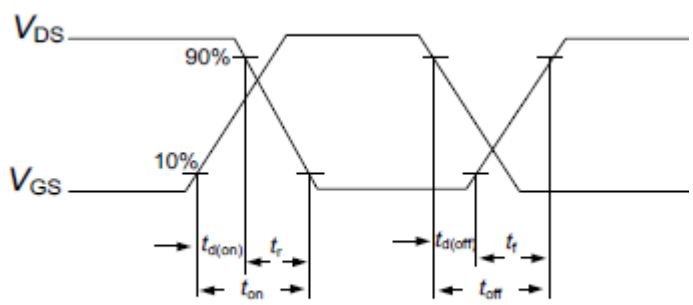
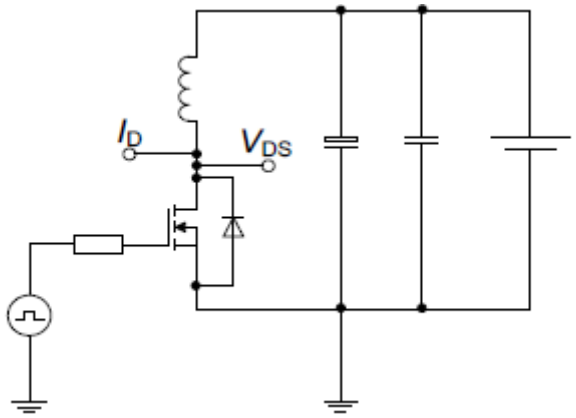
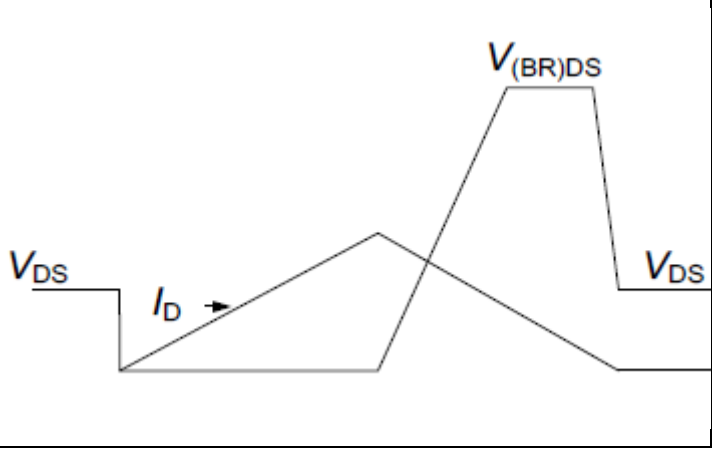
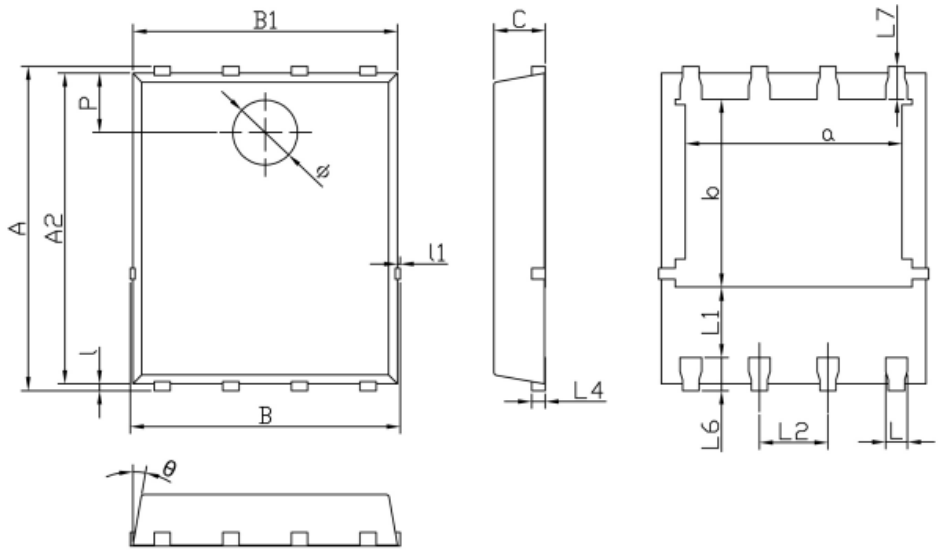
Switching times test circuit for inductive load	Switching times waveform
	

Table 9. Unclamped Inductive Load

Unclamped inductive load test circuit	Unclamped inductive waveform
	

7. Package Outlines

Figure 1 Outline DFN5*6 Dimensions in mm



Dimensions In Millimeterer			
Symbol	MIN	TYP	MAX
A	5.90	6.00	6.10
a	3.91	4.01	4.11
A2	5.70	5.75	5.80
B	4.90	5.00	5.10
b	3.37	3.47	3.57
B1	4.80	4.90	5.00
C	0.90	0.95	1.00
L	0.35	0.40	0.45
l	0.06	0.13	0.20
L1	1.10	–	–
l1	–	–	0.10
L2	1.17	1.27	1.37
L4	0.21	0.26	0.34
L6	0.51	0.61	0.71
L7	0.51	0.61	0.71
P	1.00	1.10	1.20
θ	8°	10°	12°
Φ	1.10	1.20	1.30

8. Appendix

CoolSemi Webpage: www.coolsemi.com.