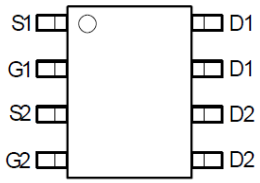
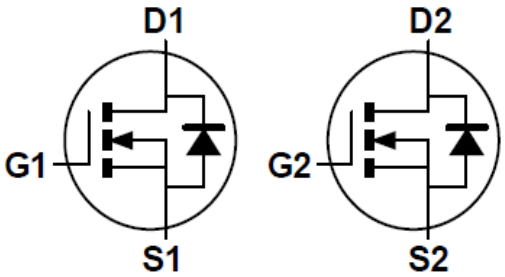
N-channel 50V, 20mΩ max.,
SGT MOSFET S2 in SOP-8

Datasheet - Production data

1. Descriptions

SOP-8	Top View
	

Schematic Diagram



Key Performance Parameters

Parameters	Value	Unit
BV_{DSS}	50	V
$R_{DS(on),max}$	20	mΩ
P_D	5.5	W
I_D	8	A

Features

- High Speed Power Switching,Logic Level
- Low Input Capacitance
- Low On-Resistance
- 100% UIS Tested
- Lead Free, Halogen Free
- Qualified for Automotive applications according to AEC-Q101.

Applications

- DC/DC Converter
- PD Charger
- Motor Driver
- Switching Voltage Regulator
- Power Management Functions

Type/Ordering Code	Package	Marking	Related Links
CSK200N05S2A	SOP-8	200N05S2A	See Appendix A

Contents

2. Maximum Ratings

at T_j = 25°C, unless otherwise specified

Absolute Maximum Ratings

Symbol	Parameter	Values			Unit	Test Condition
		Min.	Typ.	Max.		
V_{DS}	Drain-source voltage	-	-	50	V	V_{GS}=0V, I_D=250μA
V_{GS}	Gate source voltage	-20	-	20	V	static; AC (f>1 Hz)
I_D	Continuous drain current	-	-	8	A	T_C=25°C
$I_{D,pulse}$	Pulsed drain current	-	-	40	A	T_C=25°C
P_D	Power dissipation	-	-	5.5	W	T_C=25°C
E_{AS}	Avalanche energy, single pulse[1)]	-	-	81	mJ	I_D=18A; V_{DD} =50V
T_j, T_{stg}	Operating and storage temperature	-55	-	175	°C	-

3. Thermal Characteristics

Thermal Characteristics

Symbol	Parameter	Values			Unit	Test Condition
		Min.	Typ.	Max.		
R_{thJC}	Thermal resistance, junction – Case	-	-	27	°C/W	T_C = 25°C
R_{thJA}	Thermal resistance, junction - ambient[2)]	-	-	70	°C/W	T_C = 25°C

4. Electrical Characteristics

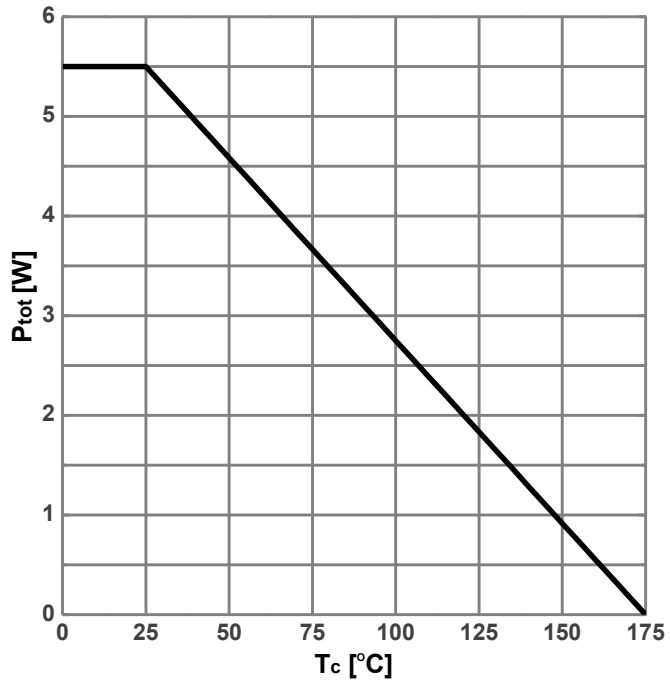
at T_j = 25°C, unless otherwise specified

Symbol	Parameter	Values			Unit	Test Condition
		Min.	Typ.	Max.		
Off Characteristics						
$V_{(BR)DSS}$	Drain-source breakdown voltage	50	-	-	V	V_{GS}=0V, I_D=250μA
I_{DSS}	Zero gate voltage drain current	-	-	100	nA	V_{DS}=50V, V_{GS}=0V
I_{GSS}	Gate-source leakage current	-	-	±100	nA	V_{GS}=±20V, V_{DS}=0V
On Characteristics[3)]						
$V_{(GS)th}$	Gate threshold voltage	1.0	-	3.0	V	V_{DS}=V_{GS}, I_D=250μA
$R_{DS(on)}$	Drain-source on-state resistance	-	16	20	mΩ	V_{GS}=10V, I_D=20A
R_G	Gate resistance	-	1.8	-	Ω	V_{DD}=0V,V_{GS}=0V,F=1MHz
g_{fs}	Transconductance		30		S	V_{DS}=5V, I_D=20A
Dynamic Characteristics						
C_{iss}	Input capacitance	-	653	-	pF	V_{GS}=0V, V_{DS}=25V, F=250KHz
C_{oss}	Output capacitance	-	110	-	pF	
C_{rss}	Reverse transfer capacitance	-	5.3	-	pF	
Switching Characteristics[4)]						
$t_{d(on)}$	Turn-on delay time	-	13	-	ns	V_{DD}=30V, V_{GS}=10V, I_D=20A,R_G=10Ω
t_r	Turn-on rise time	-	25	-	ns	
$t_{d(off)}$	Turn-off delay time	-	26	-	ns	
t_f	Turn-off fall time	-	10	-	ns	
Q_g	Gate charge total	-	12.4	-	nC	V_{DD}=30V, I_D=20A, V_{GS}=0 to 10V
Q_{gs}	Gate to source charge	-	1.5	-	nC	
Q_{gd}	Gate to drain charge	-	2.5	-	nC	
Reverse Diode Characteristics						
V_{SD}	Diode forward voltage[3)]	-	0.9	1.2	V	V_{GS}=0V, I_F=20A
I_S	Diode forward current[2)]	-	-	2.5	A	
t_{rr}	Reverse recovery time	-	38	-	ns	V_{GS}=0V, I_F=20A, di_F/dt=100A/μs[3)]
Q_{rr}	Reverse recovery charge	-	17	-	μC	

1) VDD=50V, L=0.5mH, RG=25Ω, Starting Tj=25°C.
2) Surface Mounted on FR4 Board, t ≤ 10 sec.
3) Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4) Guaranteed by design, not subject to production

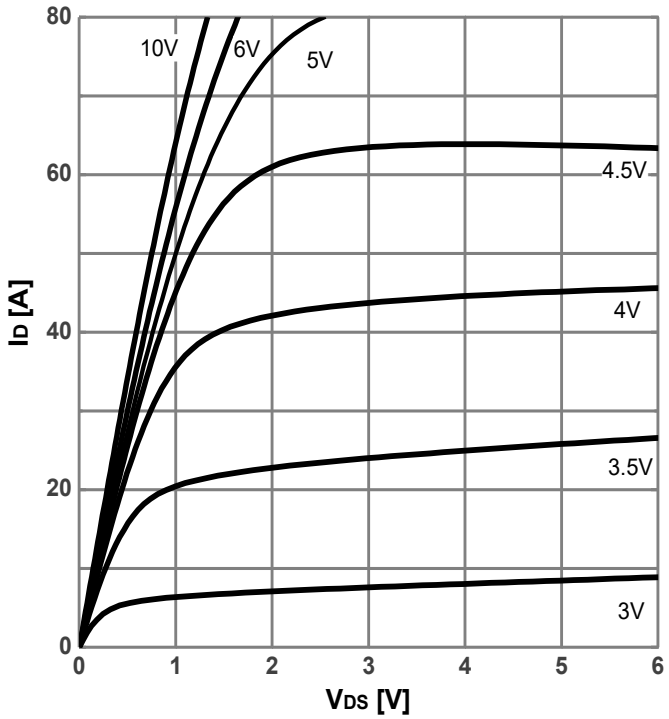
5. Electrical Characteristics Diagrams

Diagram 1: Power dissipation



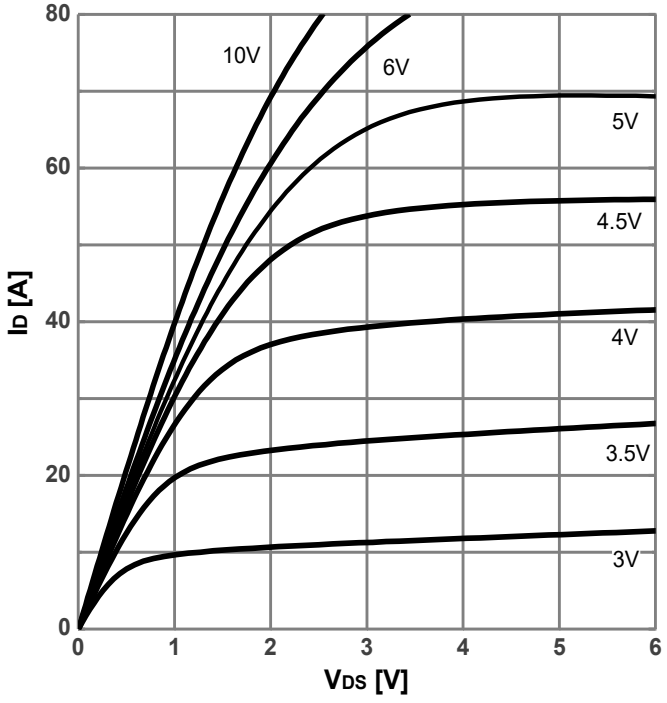
P_{tot}=f(T_C)

Diagram 2: Typ. output characteristics



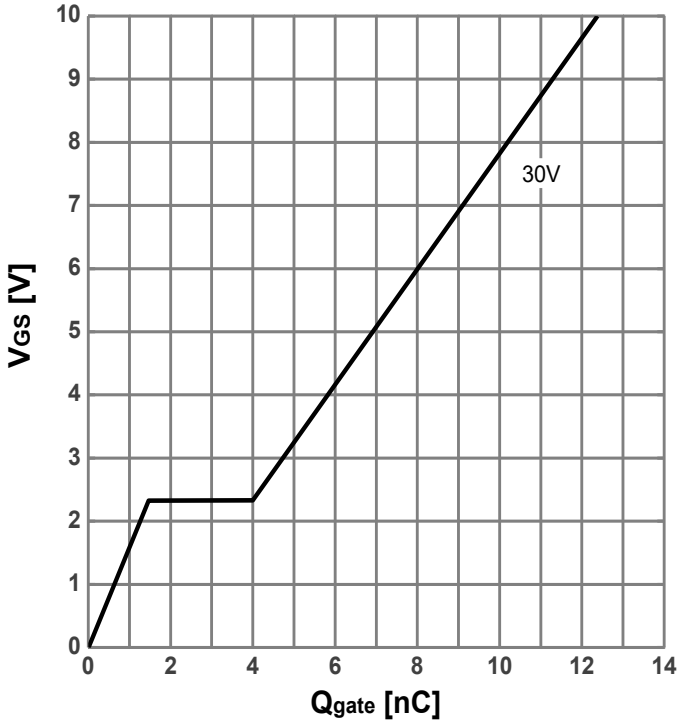
I_D=f(V_{DS}); Tj=25°C; parameter: V_{GS}

Diagram 3: Typ. output characteristics



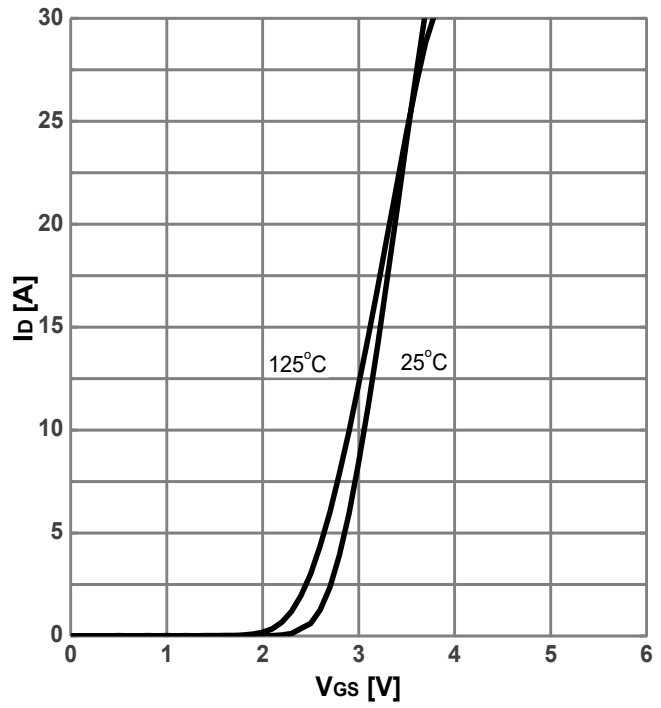
I_D=f(V_{DS}); Tj=125°C; parameter: V_{GS}

Diagram 4: Typ. gate charge



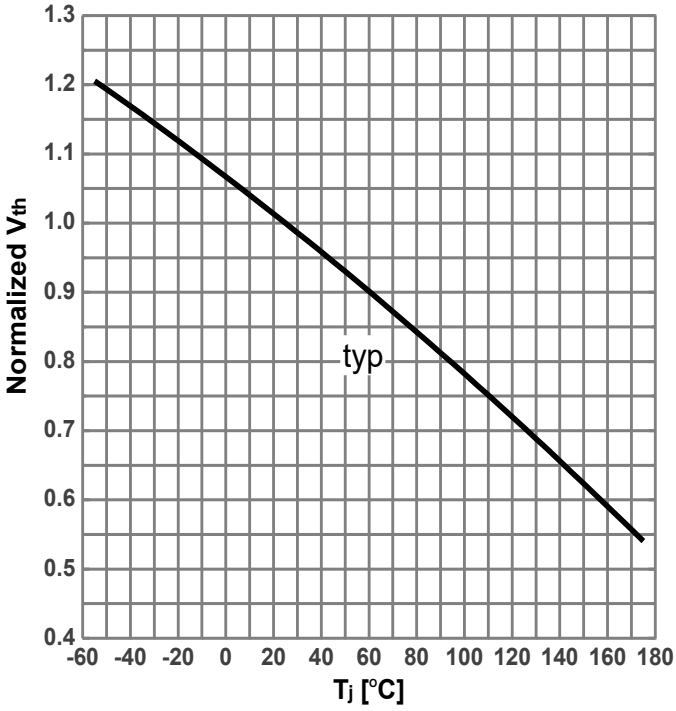
V_{GS}=f(Q_{gate}); I_D=20A pulsed; V_{DS}=30V

Diagram 5: Typ. transfer characteristics



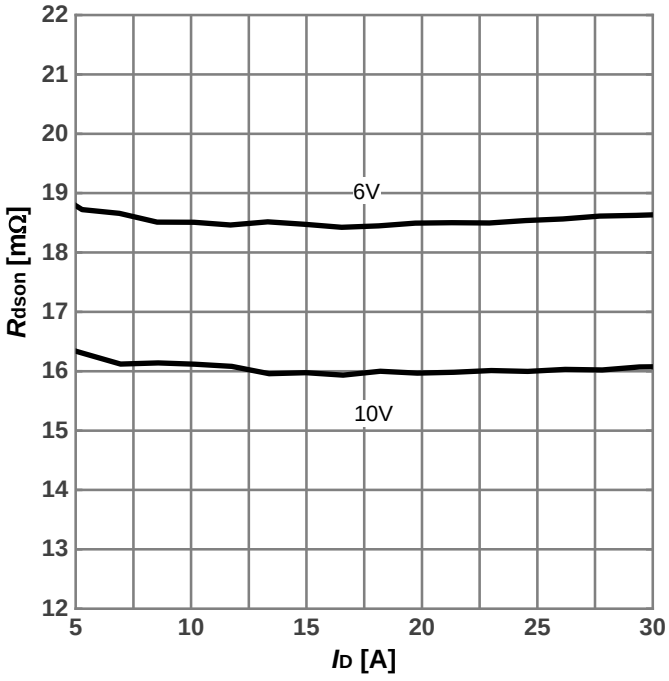
I_D=f(V_{GS}); V_{DS}=5V; parameter: T_j

Diagram 6: Gate threshold voltage vs. Junction temperature



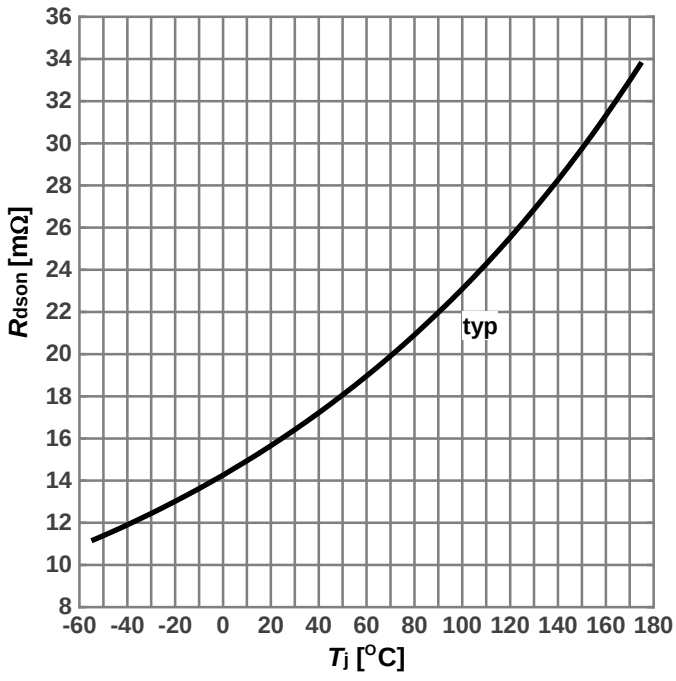
V_{th}=f(T_j); I_D=250μA

Diagram 7: On-state resistance vs. Drain current



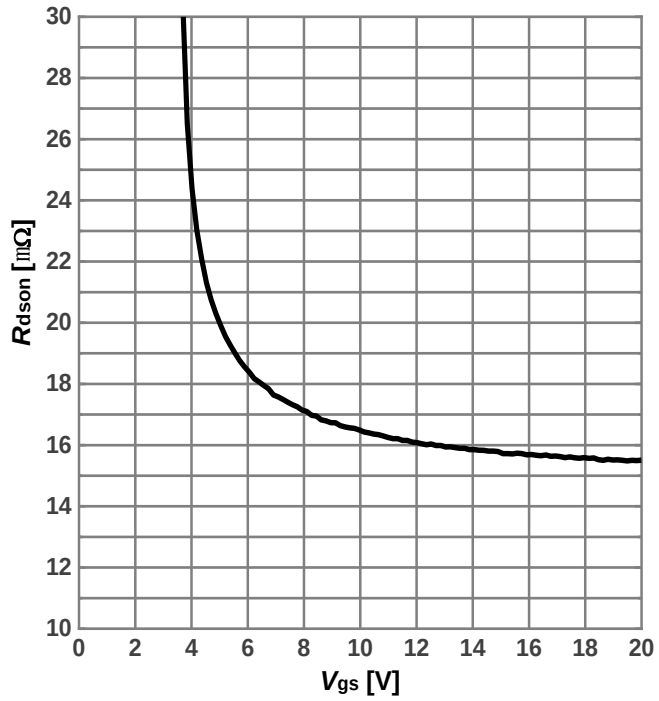
R_{DS}(on)=f(I_D); Tj=25°C; parameter: V_{GS}

Diagram 8: On-state resistance vs. Junction temperature



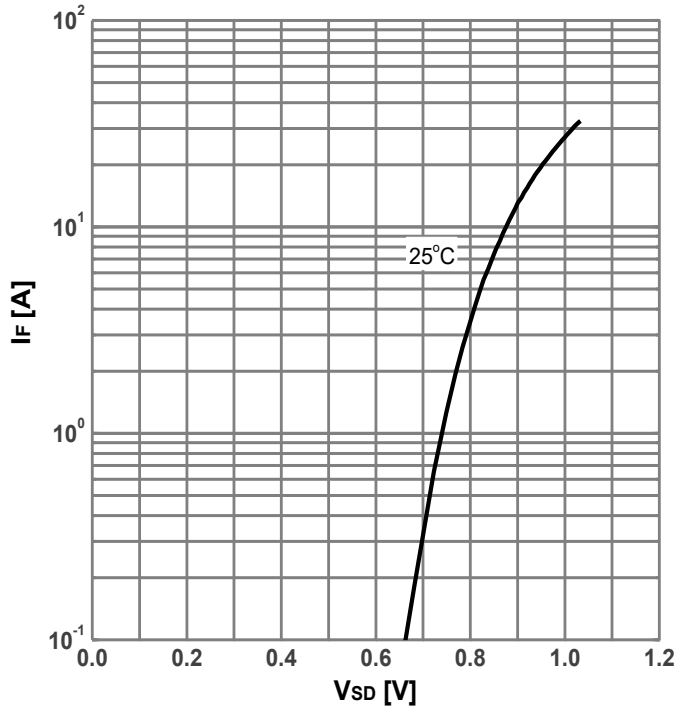
R_{DS}(on)=f(T_j); I_D=20A; V_{GS}=10V

Diagram 9: On-state resistance vs. Vgs characteristics



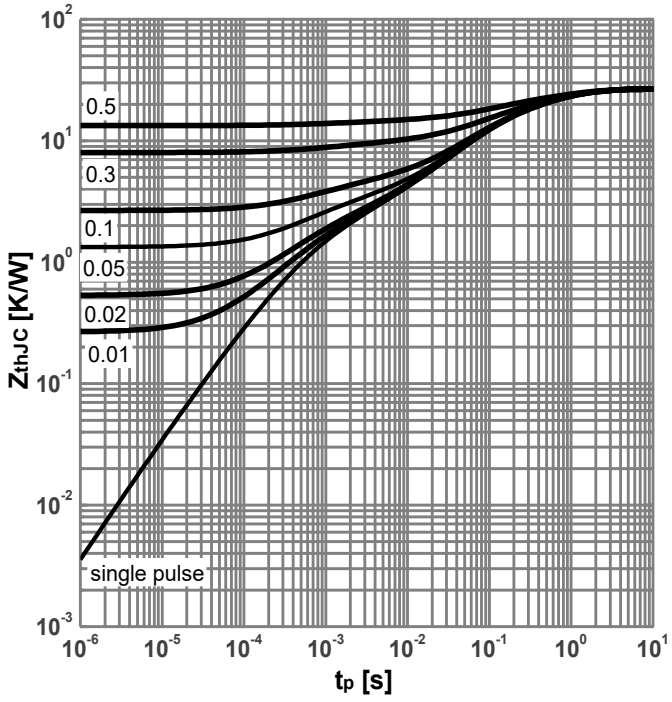
$R_{DS}(on)=f(V_{gs})$; $T_j=25°C$; $I_D=20A$

Diagram 10: Forward characteristics of reverse diode



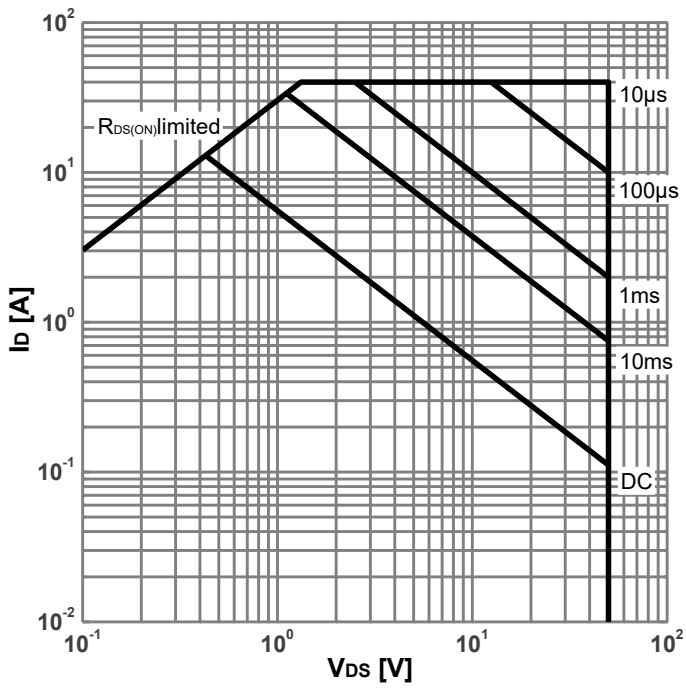
$I_F=f(V_{SD})$; parameter: T_j

Diagram 11: Max. transient thermal impedance



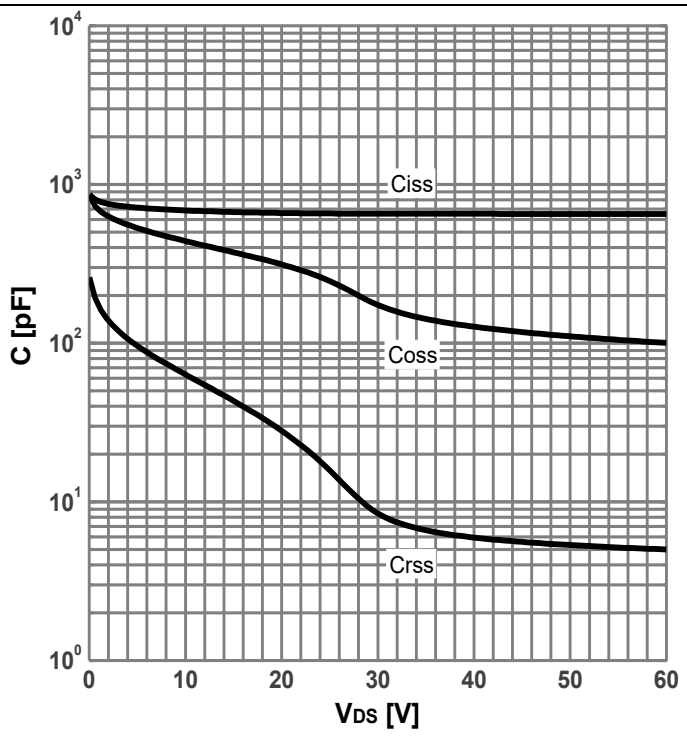
$Z_{thJC}=f(t_p)$; parameter: D= t_p/T

Diagram 12: Safe operating area



$I_D=f(V_{DS})$; $T_j=25°C$; D=0; parameter: t_p

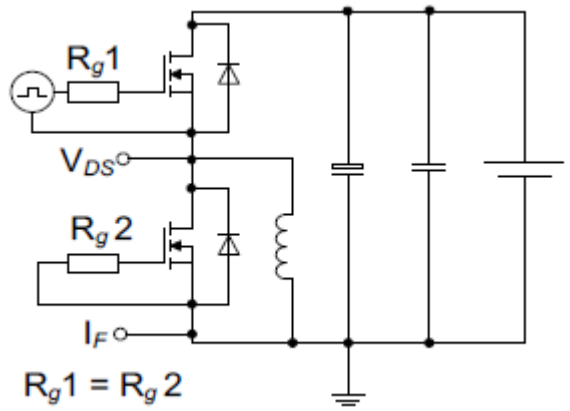
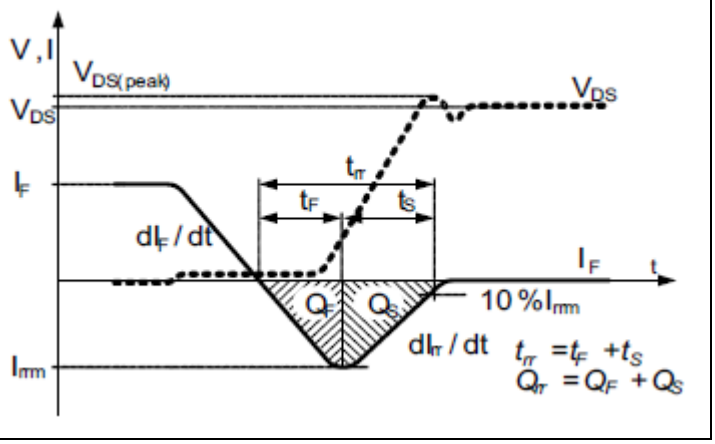
Diagram 13: Typ. capacitances



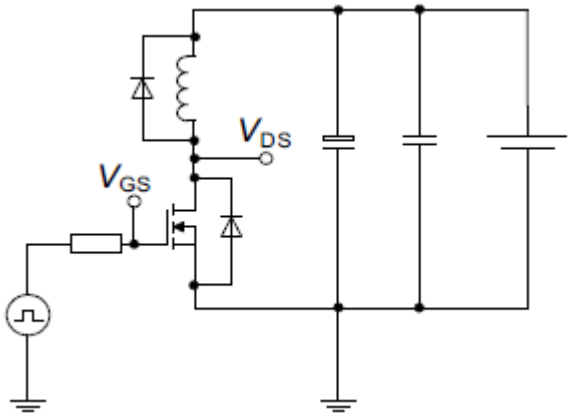
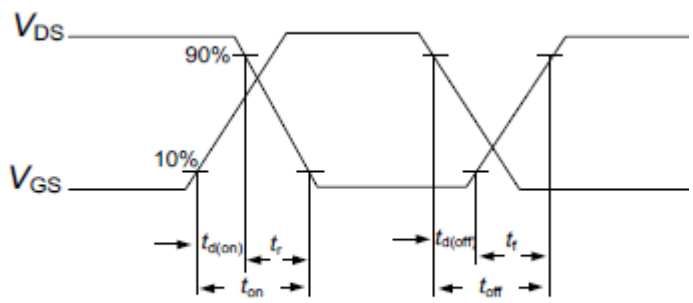
C=f(V_{DS}); V_{GS}=0V; f=250KHz

6. Test Circuits

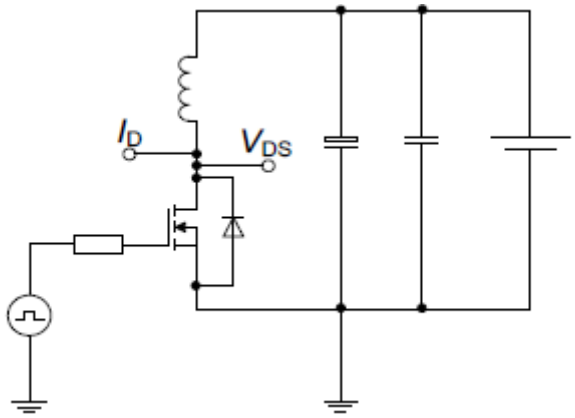
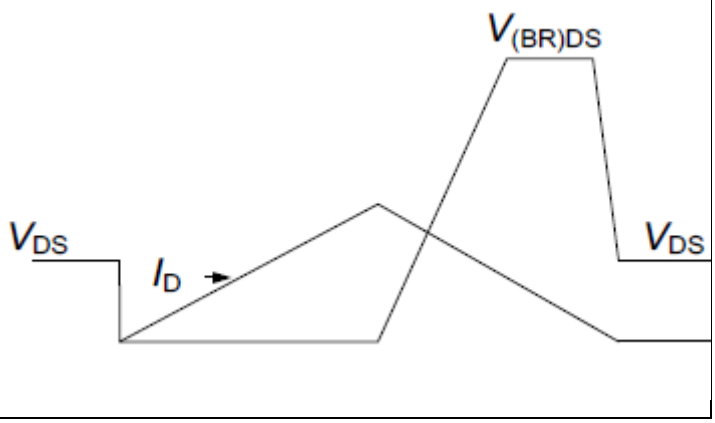
Diode Characteristics

Test circuit for diode characteristics	Diode recovery waveform
	

Switching Times

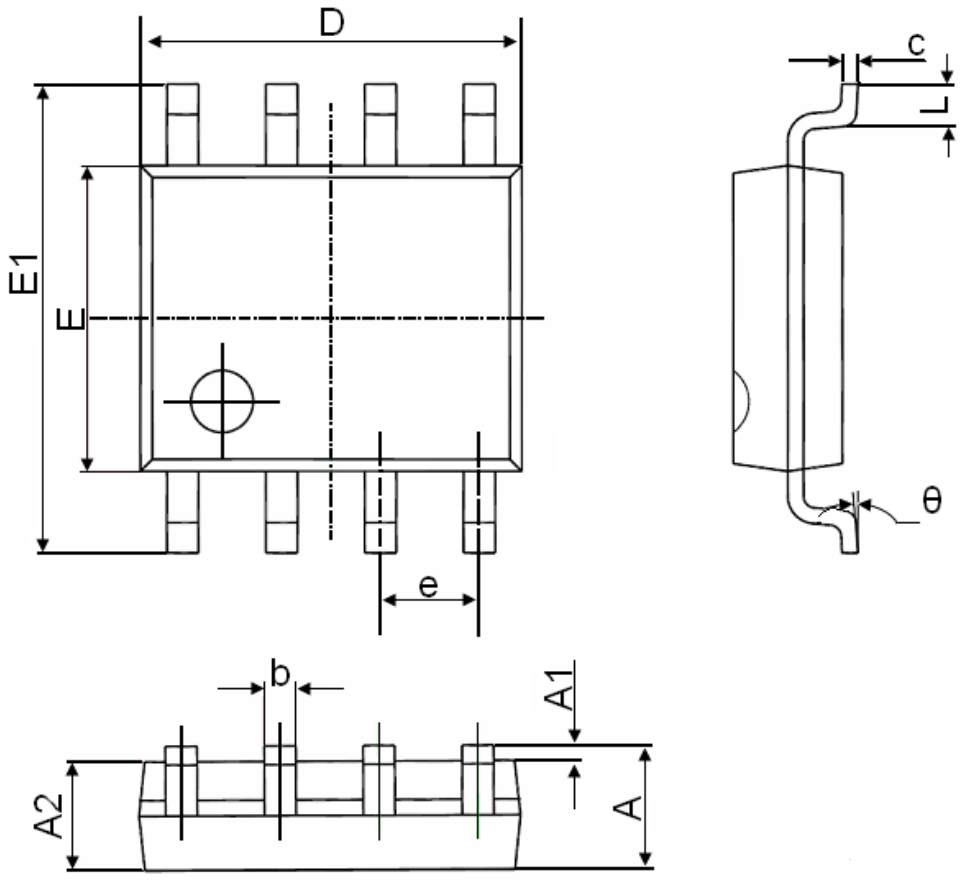
Switching times test circuit for inductive load	Switching times waveform
	

Unclamped Inductive Load

Unclamped inductive load test circuit	Unclamped inductive waveform
	

7. Package Outlines

Figure 1 Outline SOP-8 Dimensions in mm



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

8. Appendix

CoolSemi Webpage: www.coolsemi.com.