CSC100N10G1

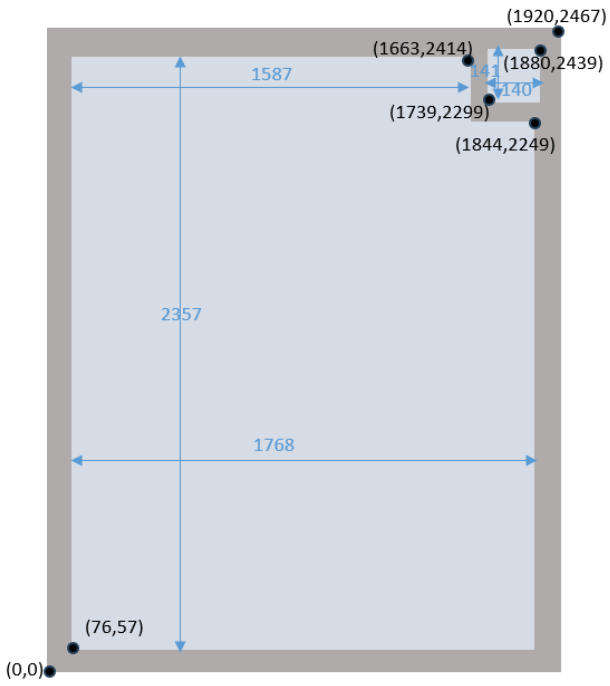
N-channel 100 V, 10.0 mΩ max., 90A
SGT Power MOSFET

Datasheet - production data

Features

- 100V, 10.0mΩ max., 90A, N-channel SGT MOSFET
- High-Frequency Switching and Synchronous Rectification in SMPS
- DC/DC in Telecoms and Industrial

Wafer Information

Chip drawing	Parameter	Value	Unit
	Wafer Size	200	mm
	Wafer Thickness	200	μm
	Chip Size	1980*2527	μm*μm
	Scribe Line Size	60	μm
	Gate Pad Size	140*141	μm*μm
	Source Pad Size	1587*2357	μm*μm
	Gross Die	5685	
	Front Metal (AlCu)	4	μm
	Back Metal (Ti/Ni/Ag)	1 / 2 / 10	KA
	Top passivation (TEOS/SIN)	4 / 6	KA

1 Absolute Characteristics

(T_C = 25 °C unless otherwise specified, TO-220 Package Reference)

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	100	V
V_{GS}	Gate-source voltage	± 20	V
I_D	Drain current (continuous) at T_C = 25 °C	90	A

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified, TO-220 Package Reference)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 250 μA, V_{GS} = 0 V	100			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 100 V, T_C=25 °C			1	μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 20 V			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 μA	1.2	1.8	2.5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 20 A		8	10	mΩ

Note

1. Product must be handled only at ESD safe workstations. Standard ESD precautions and safe work environments are as defined in MIL-HDBK-263.
2. Product must be handled only in a class 10,000 or better-designated clean room environment.
3. Proper storage conditions are necessary to prevent product contamination and/or degradation after shipment.
4. Cool Semiconductor reserves the right to modify the datasheet. Customer should get the latest specification before placing orders. If you have any questions, you can contact us to confirm.